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Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

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Developed by the JEDEC Reliability Test Methods for Packaged Devices Committee (JC-14.1) and the SMT Attachment Reliability Test Methods Task Group (6-10d) of the Product Reliability Committee (6-10) of IPC

Users of this publication are encouraged to participate in the development of future revisions.

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Mechanical Shock In-situ Electrical Metrology Test Guidelines for FCBGA SMT Component Solder Crack and Pad Crater/Trace Crack Detection

1 SCOPE

This document establishes metrology guidelines to electrically and reliably detect solder joint opens on Flip-Chip Ball Grid Array (FCBGA) SMT board assemblies during the mechanical shock or drop event. In-situ metrology can monitor not only FCBGA assembly with daisy-chain components but can also monitor product components with power or ground planes or equivalent daisy-chain test structures. In addition, the metrology is capable of providing ball-level resolution provided appropriate test structures are designed into the test package and board. The metrology was validated for thermal solutions with compression load. Although the initial focus of this metrology is specific to FCBGA assemblies in mechanical shock or drop testing, the same approach can eventually be extended to other stress tests (e.g. vibration, mechanical bend, and temperature cycle) and/or components (including other BGAs, sockets assemblies and TH/SMT leaded/leadless assemblies) depending on evolution and adoption of the guidelines (title and scope could be updated based on the outcome from future planned studies). This metrology may not be capable of detecting partial solder ball cracks, since resistance does not significantly change until the solder crack is close to 100%. Finally, the detection of pad cratering failures will be possible through use of this metrology, provided there is a complete trace crack.

1.1 Purpose This document provides:

- Description of concept behind efficient in-situ electrical metrology to reliably detect FCBGA assembly solder joint opens during mechanical shock or drop test
- Guidelines for special daisy-chain test structure to standardize test board design for ball-level electrical monitoring of FCBGA joints
- Minimum requirements to establish the metrology in the lab for execution
- Definition for in-situ electrical open detection criteria
- Guidelines for electrical and FA data analysis

1.2 Background Some of the existing metrologies, including JESD22-B110, JESD22-B11, and IPC/JEDEC-9703, do not provide in-situ electrical monitoring of FCBGA solder joint opens during test. They either rely on electrical test before and after the test or use less efficient destructive physical analysis techniques which are either not reliable (see Appendix D for false fail rate based on hand probe e-test), cost-effective, or time consuming. The proposed shock metrology provides reliable electrical data with ball-level resolution, thereby eliminating the need for further fault isolation. Finally, the metrology provides instantaneous response in display format, thereby reducing the testing throughput time with minimal to no physical destructive failure analysis needs [1]. Solder joint built-in self-test (SJ BIST) in situ metrology usage was neither demonstrated on a large scale sample size, nor was it applied on non-field programmable gate array (non-FPGA) packages [2]. Traditional daisy chain resistance measurement is usually limited by a combination of speed and channel count. In addition, the metrology does not provide ball-level resolution or cannot monitor board assemblies with real product components. Current based event detectors are more prone to noise due to poor resolution and no results display (to confirm failures) compared to voltage metrology.

1.3 Performance Classification At this point in time, the reliability requirements need to be established by agreement between customer and supplier and this document only provides guidelines on how to use in-situ test method.

1.4 Definition of Terms The definition of all terms used herein **shall** be as specified in IPC-T-50 and as defined below.

1.4.1 FCBGA package: (Flip-chip) ball grid array component (does not include connectors or sockets).

1.4.2 SMT Surface-mount technology.

1.4.3 Product Component Any functional component used in electronic industry that has ground or power planes or equivalent test structures.

1.4.4 Voltage Metrology Name of the new metrology described in this document that can detect electrical failures on product component.

1.4.5 Power Ball Ball on the FCBGA component used for voltage power.