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Design and Assembly Process Implementation for Flip Chip and Die-Size Components

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Developed by the Flip Chip Mounting Task Group (5-21g) of the
Assembly & Joining Processes Committee (5-20) of IPC

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Users of this publication are encouraged to participate in the
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Table of Contents

1 SCOPE	1	4.5.3 Solder Paste Deposition	17
1.1 Target Audience and Intent	1	4.5.4 Solder Electroplating	18
1.2 Definition of Requirements	1	4.5.5 Other Bumping Techniques and Materials	18
1.3 Classification of Product	1	4.6 Ball and Bump Terminal Process for Flip Chip	18
2 APPLICABLE DOCUMENTS	1	4.6.1 Dimensional Control	18
2.1 IPC	1	4.6.2 Metallurgical Integrity	19
2.2 Joint Industry Standards	2	4.6.3 Cleanliness of Bumping Site	19
2.3 JEDEC	3	4.7 Surface Redistribution	19
3 REQUIREMENTS AND TECHNOLOGY OVERVIEW	4	4.8 Cu Post or Pillar Termination	20
3.1 Terms and Definitions	4	5 FLIP CHIP POST-FABRICATION PROCESSING	20
3.1.1 Acronyms and Abbreviations	4	5.1 Test and Reliability Screening	20
3.2 History of Flip Chip Mounting	4	5.1.1 Known Good Die (KGD)	20
3.2.1 Advantages of Flip Chip Mounting	5	5.1.2 Known Quality Die (KQD)	20
3.3 History of Die Size and Chip Scale Array Packaging	5	5.1.3 Wafer Test and Equipment Challenges/Concerns	20
3.3.1 Film-Based Package Substrate	6	5.1.4 Reliability Screening at the Wafer or Die Level	21
3.3.2 Commercial Package Variations	7	5.2 Wafer Thinning (Grinding and Polishing)	22
3.3.3 Redistribution	7	5.2.1 Thinning and Polishing Process	22
3.3.4 Advantages of Die-Size Package and Chip Scale Package (CSP) Technology	7	5.2.2 Processing Effect on the Quality of the Die	22
4 FLIP CHIP TECHNOLOGY	8	5.3 Singulation	22
4.1 Electrical Design Considerations	8	5.3.1 Sawing	22
4.1.1 Equivalent Circuitry	8	5.3.2 Scribe and Break	23
4.1.2 Final Metal Traces	9	5.4 Laser Sawing	24
4.1.3 Inductance and Capacitance	10	5.4.1 Wafer Dicing With Deep Reactive-Ion Etching (DRIE) Process	24
4.1.4 High-Frequency Performance	10	5.5 Shipping and Handling	24
4.2 Thermal Design	10	6 FLIP CHIP INTERCONNECTING SUBSTRATES	25
4.2.1 Bump Interconnect Thermal Model	11	6.1 Substrate Base Material	25
4.3 Flip Chip Preparation for Mounting	12	6.1.1 Flexible Base Substrates	25
4.3.1 Design Guide Check List	12	6.1.2 Reinforced-Resin Substrates	26
4.3.2 Final Metal	14	6.1.3 Cu Conductor Base Metals for Flexible and Reinforced Laminates	26
4.3.3 Surface Passivation	14	6.1.4 Ceramic Substrates	26
4.3.4 Footprint Population	15	6.1.5 Si-Based Substrates	27
4.4 Design Output Requirements	16	6.2 Surface Finish Properties	28
4.4.1 Final Metal Reticle Mask	16	6.2.1 Chemical Plating Finishes (Electrolytic and Electroless)	28
4.4.2 Passivation (Terminal Via) Reticle Mask and Plan	16	6.2.2 Thick-Film Metallic Finishes	28
4.4.3 Unit Cell Design	16	6.2.3 Thick-Film Deposition Processes	28
4.5 Land Pattern Design	17		
4.5.1 Land Pattern for Ceramic Substrate Design	17		
4.5.2 Solder Bumping	17		

6.2.4	Sputtered (Thin-Film) Conductive Finishes	28	7.6	Contact Array Redistribution	40
6.2.5	Sputtered Metal Deposition Process	28	7.6.1	Staggered-Array Planning	40
6.3	Alternative Circuit Forming Processes	28	7.6.2	Die Shrink Considerations	41
6.3.1	Laser Direct Image (LDI)	28	7.7	Flip Chip and Chip Scale Package (CSP) Assembly	41
6.3.2	Inkjet Imaging	29	7.7.1	Passivation Material Requirements	41
6.3.3	Silkscreen and Stencil Printing	29	7.7.2	Requirements for Bump and Ball Terminal Alloy	41
6.3.4	Direct Image Conductive Inks Process	29	7.7.3	Flux for Flip Chip and Chip-Size Package Mounting	42
7	PACKAGE-LEVEL STANDARDIZATION	30	7.7.4	Solder Paste for Flip Chip and Chip- Size Package Mounting	42
7.1	Controlling Physical Features	30	7.7.5	Electrically Conductive Adhesives for Flip Chip Attachment	42
7.2	Mechanical Outline Standards for Die-Size Ball Grid Array (DSBGA) Packaging	30	7.7.6	Underfill Material Requirements	42
7.2.1	JEDEC Standard for Die-Size BGA (DSBGA)	31	7.7.7	Encapsulation Material Requirements	43
7.2.2	Ball Terminal Measurement	32	7.8	Flip Chip and Chip Scale Assembly Performance Requirements	43
7.2.3	Die-Size Ball Grid Array (DSBGA) Outline Consideration	32	7.8.1	Thermal Cycle Stress Testing of Soldered Assemblies	43
7.3	Electrical Performance Planning	32	7.9	Trays for Flip Chip and Chip-Size Packages (Shipping and Delivery)	43
7.3.1	Modeling and Simulation	33	8	SYSTEM-LEVEL ISSUES	44
7.3.2	Electromagnetic Radiation	33	8.1	Design for Assembly	44
7.3.3	Electrical Bias Created by Nonelectrical Phenomena	33	8.1.1	Flip Chip, Die-Size Ball Grid Array (DSBGA) Land Pattern Design	44
7.4	Standards for Package-Level Substrate Design and Performance	33	8.1.2	Component Clearance	45
7.4.1	Qualification and Performance of Organic Structures for Flip Chip Mounting	33	8.1.3	Rigid Organic Substrate Design	45
7.4.2	Qualification and Performance for Organic Single and Multichip Mounting and Interconnecting Structures	33	8.1.4	Restriction of Hazardous Substances (RoHS)-Compliant Surface Finish Selection	47
7.4.3	Qualification and Performance Standard for Inorganic Mounting Structures	34	8.2	Flexible Circuit Substrate Design	48
7.4.4	Test Methods for Qualification and Evaluation of Flip Chip Mounting Structures	34	8.2.1	Material for Harsh Environments	48
7.4.5	Mechanical Performance Test Requirements	34	8.2.2	Rigid-Flex Substrates	48
7.5	Flip Chip Development and Performance Standards	34	8.3	Ceramic Substrate Design	49
7.5.1	Flip Chip Integrated Circuit (IC) Component Design	34	8.3.1	Thick-Film on Ceramic Substrates	49
7.5.2	Wafer Fabrication and Bond Site Planning	35	8.3.2	Thin Film on Ceramic Substrates	50
7.5.3	Wafer-Level Terminal Forming Methodologies	35	8.3.3	Multiple-Layer Ceramic Substrates	50
7.5.4	Molded Feed-Out Wafer-Level Process (MFWL)	36	8.4	Substrate Design Guide Checklist	51
7.5.5	Design Standards for Wafer-Level Ball Grid Array (WLBGA)	36	9	FLIP CHIP AND DIE-SIZE DEVICE ASSEMBLY	51
7.5.6	Bond Pad and Array Planning	37	9.1	Substrate Preparation	51
7.5.7	Critical Factor: Bump Attachment and Bonding	39	9.2	Flip Chip and Die-Size Device Placement	51
7.5.8	Metallurgical Integrity	39	9.3	Attachment Processes	52
			9.3.1	Solder Attachment Process for Flip Chip	52
			9.3.2	Reflow Soldering	52
			9.3.3	Solder Alloys and Process Parameters	52
			9.3.4	Solder Stencil Development	53

9.4	Solder Process Profile Planning	54	10.8.2	Solder Interface Grain Structure Effects	67
9.4.1	Reflow Process Implementation	55	10.8.3	Global Expansion Mismatch	68
9.4.2	Solder Process Evaluation	55	10.8.4	Local Expansion Mismatch	68
9.5	Thermocompression and Ultrasonic Bonding ...	56	10.8.5	Internal Expansion Mismatch	68
9.6	Adhesive Interconnection	56	10.8.6	Solder Attachment Failure	68
9.6.1	Anisotropic Conductive Adhesives	56	11	RELIABILITY PREDICTION MODELING	68
9.6.2	Isotropic Conductive Adhesives	57	11.1	Large Temperature Excursions	69
9.6.3	Nonconductive Adhesive Process	57	11.2	Creep-Fatigue Modeling Creep	69
9.7	Cleaning	57	11.3	Statistical Failure Distribution and Failure Probability	69
9.7.1	No-Clean Flip Chip Processes	57	11.4	Damage Modeling	69
9.7.2	Aqueous Flip Chip Cleaning Technology	57	12	VALIDATION AND QUALIFICATION TESTING ...	70
9.8	Attachment Assessment	58	12.1	Screening Procedures	70
9.8.1	Optical Inspection	58	12.2	Evaluating Solder Joints	70
9.8.2	X-Ray Inspection	58	12.3	Testing Scenarios	70
9.9	Underfill (Flip Chip Encapsulation)	58	12.3.1	Critical Environmental Testing	70
9.9.1	Capillary Flow Underfill Process Overview	59	12.3.2	Die Testing on Known Good Die (KGD)	70
9.9.2	Fluxing (No Flow) Underfill	59	12.4	Inspection and Process Control Assurance	71
9.9.3	Removable/Reworkable Underfill	60	12.5	Total Quality Management and Manufacturing (TQMM)	71
9.9.4	Substrate Surface Compatibility	60	13	SUPPLY CHAIN ISSUES	71
9.10	Electrical Test	60	13.1	Supply Chain Traceability	71
9.11	Rework and Repair	60	13.2	Configuration Management	71
9.11.1	Hot-Air Process for Device Removal	60	APPENDIX A	Glossary	72
9.11.2	Laser Process for Device Removal	61	APPENDIX B	Acronyms	78
10	REQUIREMENTS FOR BOARD- AND MODULE-LEVEL RELIABILITY	61			
10.1	Robustness of Products to Use	61			
10.2	Chip Scale Package Robustness and Reliability	61			
10.3	Reliability Factors	63			
10.3.1	Wear-Out Failures	63			
10.3.2	Creep	63			
10.3.3	Electromigration	63			
10.3.4	Corrosion	63			
10.3.5	Thermomigration	64			
10.4	Solder Bump Mechanical Reliability	64			
10.4.1	Strain	64			
10.4.2	Effect of Thermal Expansion Mismatch	64			
10.4.3	Temperature Cycling Frequency	65			
10.5	Wear-Out Mechanisms	65			
10.5.1	Reliability Factors	65			
10.5.2	Benefits of Reinforcement	66			
10.6	Event-Related Failures	66			
10.7	Design for Reliability (DFR)	66			
10.8	Damage Mechanisms and Failure of Solder Attachments	66			
10.8.1	Solder Joints and Attachment Types	67			

Figures

Figure 3-1	Solid Copper Core Ball Contact	4
Figure 3-2	Flip Chip With a Ag-Coated Cu Core Terminal to Maintain Uniform Stand-Off Height	4
Figure 3-3	Solder-Bumped Wafer-Level Ball Grid Array (WLBGA)	5
Figure 3-4	Array-Configured Die-Size Ball Grid Array (BGA)	5
Figure 3-5	Face-Down Mounted Die (Flip Chip) on Organic Substrate	6
Figure 3-6	Face-Up Wire-Bond Chip Scale Package (CSP)	6
Figure 3-7	Narrow Opening in a Substrate Provides Access for Through-Window Wire-Bond Process	6
Figure 3-8	Commercial Flip-Chip and Wafer-Level Semiconductor Package Innovations	7
Figure 3-9	Wire-Bond Pad to Array Redistribution Provides Wider Spacing and Larger Terminal Features	7

Figure 4-1	Bump Equivalent Circuit (Redistributed Chip) ..	8	Figure 5-8	Horizontal and Vertical Carriers for Transporting Wafers	25
Figure 4-2	Solder Bump Electrical Path (Redistributed Chip)	9	Figure 6-1	Low Input/Output (I/O) Flip Chip Device With Solder Bump Terminals	26
Figure 4-3	Final Metal Trace and Underlying Traces (Cross-Section)	10	Figure 6-2	High Input/Output (I/O) Flip Chip on Multilayer Ball Grid Array (BGA)	27
Figure 4-4	Thermal/Electrical Analogy	11	Figure 6-3	Laser Direct Imaging (LDI)	28
Figure 4-5	Bump Interconnect Equivalent Model	11	Figure 6-4	Offset-Printed Conductive Ink Pattern	29
Figure 4-6	Alignment to Visual/Sensitive Chip Structure	13	Figure 7-1	Die-Size Ball Grid Array (BGA) Package Examples	30
Figure 4-7	Minimum Pitch From Solder Bump to Passivation Seal	13	Figure 7-2	Die-Size Ball Grid Array (DSBGA) Package Outline Showing a Fully Populated Terminal Array (Bottom View)	31
Figure 4-8	Comparing Perimeter and Redistributed Terminal Sites	14	Figure 7-3	Ball Coplanarity	32
Figure 4-9	Redistribution of a Single Metal Layer Device	14	Figure 7-4	Terminal Depopulation From the Full Array ...	32
Figure 4-10	Passivation Cross-Section	14	Figure 7-5	Flip Chip Fan-Out on Substrate	34
Figure 4-11	Suggested Distribution of Redundant Bump Terminals	15	Figure 7-6	Comparing Perimeter Wire Bond Pad Layout Variations	35
Figure 4-12	Array Design Anticipating the Potential for Die Shrink	15	Figure 7-7	Comparing Wafer-Level Terminal Formation Methodologies	35
Figure 4-13	Signal and Power Distribution Positions	15	Figure 7-8	Molded Fan-Out Wafer-Level Process (FOWLP) Sequence	36
Figure 4-14	Nested I/O Terminals	16	Figure 7-9	Uniform Terminal Array Is a Result of Surface Redistribution	36
Figure 4-15	Typical Bump Passivation Reticle Mask Format for Peripheral and Array Terminal Variations	16	Figure 7-10	Fully Populated Array Matrix With Corner A1 ¹ Mark on the Outer Surface of the Die (Top View Left, Bottom View Right)	37
Figure 4-16	Product Unit Cell Plan	16	Figure 7-11	Comparing Passivation Patterns	39
Figure 4-17	Comparing Solder Ball Collapse After Reflow	17	Figure 7-12	Redistribution of Perimeter Bond Pads Into a Raised-Array Terminal Pattern	40
Figure 4-18	Land Pattern Planning for Flip Chip Attachment on a Ceramic-Based Substrate	17	Figure 7-13	Wafer-Level Ball Grid Array (WLBGA) Design Layout Guideline for a Staggered-Array Pattern	40
Figure 4-19	Mass Reflow Solder Bumping of the Die While in a Wafer Format	17	Figure 7-14	Terminal Array Accommodating Die Shrink ...	41
Figure 4-20	Au Stud-Bump Terminal Comparing a Wire Break-Off to a More Uniform Cut-Wire Profile	18	Figure 7-15	Underfill Material Applied to Mechanically Stabilize the Flip-Chip-Mounted Die	42
Figure 4-21	Surface Redistribution Layer of the Bond Sites to a Uniform Electroplated Bump Terminal Array	19	Figure 7-16	Encapsulation Material Dispensing	43
Figure 4-22	Solder-Capped Cu Power Pillar Terminal	20	Figure 7-17	JEDEC Standard Carrier Tray Designed for Array-Packaged Devices	43
Figure 5-1	Wafer-Level Testing Identifies Die Elements That Do Not Meet Established Functional Criteria	21	Figure 7-18	Tray Carrier With Smaller Partitions	44
Figure 5-2	Groove-Cutting and Wafer-Thinning Process Flow for Low Stress Die Singulation	23	Figure 8-1	Sequential Build-Up Substrate Structure	45
Figure 5-3	Scribe and Break Singulation	23	Figure 8-2	Flip-Chip and SMT Mounted Onto a Rigid-Flex Substrate	48
Figure 5-4	Scribe and Break Singulation Aspect Ratio Consideration	23	Figure 8-3	Ceramic-Based Substrates	49
Figure 5-5	Thin Wafer	24	Figure 8-4	Flip Chip and SMT on a Ceramic-Based Substrate	49
Figure 5-6	Example Street Formed in Wafer Using the Deep Reactive-Ion Etching (DRIE) Process ..	24	Figure 8-5	Three-Layer, Low-Temperature Cofired Ceramic Substrate	50
Figure 5-7	Basic Die Singulation Process Using Deep Reactive-Ion Etching (DRIE) Ablation Process	24	Figure 9-1	Automated Placement System	51
			Figure 9-2	Flip Chip Attachment Process Using Flux Dipping of Terminals	52
			Figure 9-3	Laser-Cut Stencil Aperture	54
			Figure 9-4	Pb-Free Solder Process Profile	54

Figure 9-5 Reflow Solder of Flip Chip Die With Discrete SMT Devices 55

Figure 9-6 Comparison of SnPb and SAC Ball-to-Package Interface 55

Figure 9-7 Direct Die Attachment Using Solid-Au Bump 56

Figure 9-8 Comparison of Flip Chip Reflow Solder Attachment and Anisotropic Adhesive Joining Process 57

Figure 9-9 System for Evaluating Perimeter Terminal Site Interface 58

Figure 9-10 Edge-Dispensed Underfill 59

Figure 9-11 Component Spacing for Tool Access 60

Figure 9-12 Hot-Air Process for Device Removal 60

Figure 10-1 Cross-Section of Crack Formation Due To Coefficient of Thermal Expansion (CTE) Mismatch 64

Figure 10-2 Effects of Accumulating Fatigue Damage in Solder Joint Structures 67

Tables

Table 3-1 Comparative Table of Various Technologies for a 100 Lead 10x10 mm Die 5

Table 4-1 Final Metal Signal Trace (30 μm) Resistances (Example) 9

Table 4-2 Final Metal Power Trace (60 μm) Resistances (Example) 9

Table 4-3 Typical Thermal Resistance for Variable Bump Options (Triple Layer Chip) 11

Table 4-4 Terminal Via and Final Metal Via Pitch 13

Table 4-5 Contact Pitch, Ball Size to Land Pattern Approximation (μm) 17

Table 5-1 Bare Die Testing Levels 20

Table 7-1 JEDEC Standard Terminal Pitch (e) and Terminal Diameter (b) Variations for Die-Size Ball Grid Array (DSBGA) (mm) 31

Table 7-2 Maximum Permitted Matrix Sizes (mm) for Recommended Body Sizes for WLBGA Packages 38

Table 7-3 Comparing Wafer-Level Ball Grid Array (WLBGA) Terminal Pitch to Ball or Bump Terminal Diameter Range 38

Table 7-4 Nominal Ball or Bump Diameter and Minimum Land Diameter for Wafer-Level Ball Grid Array (WLBGA) 39

Table 8-1 Ball and Land Pattern Size Comparison 44

Table 8-2 Substrate Design Feature Characteristics 45

Table 8-3 IPC-4101 RoHS-Compliant Substrate Materials 47

Table 8-4 Physical Attributes of Nonreinforced Polyimide Films 48

Table 8-5 Thin-Film Circuit on Ceramic-Based Substrates 50

Table 9-1 Solder Alloy Examples 53

Table 10-1 Product Categories and Use Environments 62

Table 10-2 Coefficient of Thermal Expansion (CTE) for Typical Materials 64

Table 10-3 Typical Heights (Joined) 64

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Design and Assembly Process Implementation for Flip Chip and Die Size Components

1 SCOPE

This document describes the design and assembly challenges for implementing flip chip technology in a direct chip attach (DCA) assembly. The effect of bare-die or die-size components in a flip chip format has an impact on component characteristics and dictates the appropriate assembly methodology. This standard focuses on design, assembly methodology, critical inspection, repair and reliability issues associated with flip chip and die-size package technologies, including wafer-level ball grid array (WLBGA).

1.1 Target Audience and Intent The target audiences for this document are managers, design and process engineers as well as operators and technicians who deal with electronic assembly, inspection and repair processes. The intent is to provide useful and practical information to those who mount bare-die or die-size components in a DCA assembly or those who are considering flip chip process implementation.

1.2 Definition of Requirements The imperative form of action verbs is used throughout this document to identify acceptance requirements that may require compliance, depending on the Performance Classification of the hardware (see 1.3). To assist the User, these action verbs are in bold text.

- a) The words “**shall/shall not**” are used whenever a requirement is intended to express a provision that is mandatory. Deviation from a **shall** or **shall not** requirement for a Performance Class may be considered if sufficient technical rationale/objective evidence is supplied to the User to justify the exception.
- b) The word “should” is used whenever a requirement is intended to express a provision that is nonmandatory and which reflects general industry practice and/or procedure.

1.3 Classification of Product The following is a general explanation of the three classes of hardware, (see J-STD-001 for details concerning the specific requirements for each of these classes).

IPC CLASS 1, General Electronic Products – Includes products suitable for applications in which the major requirement is function of the completed assembly.

IPC CLASS 2, Dedicated Service Electronic Products – Includes products for which continued performance and extended life is required and for which uninterrupted service is desired, but not critical. Typically, the end-use environment would not cause failures.

IPC CLASS 3, High-Performance Electronic Products – Includes products for which continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Each of these three classes most likely will have different reliability requirements as dictated by the end user and the intended use environment.

2 APPLICABLE DOCUMENTS

2.1 IPC¹

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-A-610 Acceptability of Electronic Assemblies

1. www.ipc.org