

IPC-7091A

2023 - January

Design and Assembly Process Implementation of 3D Components

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June 2017

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Developed by the 3D Electronic Packages Guideline Task Group (B-11a)
of the Packaged Electronic Components Committee (B-10) of IPC

Supersedes:
IPC-7091 - June, 2017

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Contact:

IPC
3000 Lakeside Drive, Suite 105 N
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

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Acknowledgment

Any document involving a complex technology draws material from a vast number of sources across many continents. Shown below are the principal members of the 3-D Electronic Packages Subcommittee (B-11a) of the Packages Electronic Components Committee (B-10). It is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Packaged Electronic Components Committee	3D Electronic Packages Guideline Task Group	Technical Liaisons of the IPC Board of Directors
Chair Vern Solberg Solberg Technical Consulting	Co-Chair Dudi Amir Intel Corporation	Bob Neves Microtek (Changzhou) Laboratories

3D Electronic Packages Guideline Task Group

Dudi Amir Intel Corporation	Dennis Fritz MacDermid Enthone Electronics Solutions	Chen Qin Suzhou Funow Company Limited
Erik Bjerke BAE Systems	Ife Hsu Intel	Jagadeeswarar Dhakrishnan Intel Corporation
Michael Carano RBP Chemical Technology, Inc.	Leo Huang APCB Electronics (Thailand) Co., Ltd	Jeff Snake ASM Assembly Systems
Zhiman Chen ZHUZHOU CRRC TIMES ELECTRIC CO., LTD	Jennie Hwang H-Technologies Group	Jose Servin Olivares Vitesco Technologies Automotive Cuautia, S.A. de C.V.
Robert Cooke NASA Johnson Space Center	Russell Kido Practical Components, Inc.	Vern Solberg Solberg Technical Consulting
Francesco Di Maio GESTLABS S.r.l.	Robert Kinyanjui John Deere Electronic Solutions	Bhanu Sood NASA Goddard Space Flight Center
Don Dupriest Lockheed Martin Missiles & Fire Control	Maurice LeBlond AI Technologies, Inc.	Pietro Vergine Advanced Rework Technology Ltd
Michael Durkan Mentor Graphics Corporation	Steve Marcell Norton ASYMTEK	Jack Zhu Veoneer China CO.,LTD
Symon Franklin Custom Interconnect Ltd	Gustaf Martensson Mycronic AB	Jinkui Zhu QingDao Coreda Intelligent Electric Co., Ltd.
	Keith Peterson Missile Defense Agency	

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Table of Contents

1	SCOPE	1	3.3	Embedded Circuitry Technology	9
1.1	Purpose	1	3.4	Advanced Packages	9
1.1.1	Target Audience	1	4	DEVICE CONSIDERATIONS	10
1.1.2	Intent	1	4.1	Package Assembly Variations	10
1.2	Classification	1	4.1.1	Die Stack (Wire Bond)	10
1.3	Measurement Units	1	4.1.2	Package-on-Package (PoP) Technologies	11
1.4	Use of “Lead”	1	4.1.3	Through Mold Via (TMV)	11
1.5	Abbreviations and Acronyms	1	4.1.4	Through-Mold Interconnect (TMI)	12
1.6	Terms and Definitions	2	4.1.5	High-Density Package-on-Package (PoP)	12
1.6.1	Die	2	4.1.5.1	Cu Pillar Interconnect (C-PI)	12
1.6.2	Electronic Element	2	4.1.5.2	Micro-Pillar (μPILR)	13
1.6.3	Interposer	2	4.1.5.3	Bond Via Array (BVA)	13
1.6.4	Substrate	2	4.1.5.4	Direct-Bond Interconnect (DBI)	13
1.6.5	Electronic Package	2	4.1.6	Folded Stack Packaging	14
1.6.6	Electronic Module	2	4.1.7	Package-on-Package Interposer (PoPi)	14
1.6.7	Three-Dimensional (3D) Packaging	2	4.1.8	Thin Small Outline Package (TSOP) Stacking	15
1.7	Implementation Challenges	2	4.1.9	High Band Memory (HBM)	15
2	APPLICABLE DOCUMENTS	3	4.1.9.1	Silicon Bridge Interposer	15
2.1	IPC	3	4.1.9.2	Embedded Multi-Die Interconnect Bridge (EMIB)	15
2.2	Joint Industry Standards	4	4.1.10	Die/Wafer Stack Cu-to-Cu	16
2.3	JEDEC	4	4.1.10.1	Cu-Sn-Cu Fusion Bond	16
2.4	Government Electronics and Information Technology Association (GEIA)	4	4.1.10.2	Thermocompression Bonding	17
3	GENERAL DESCRIPTION	4	4.1.10.3	Adhesion Bonding	18
3.1	Technology Overview	4	4.1.11	Three-Dimensional (3D) Interposer/Substrate Packaging	18
3.1.1	Die Stack Package	5	4.2	General Requirements	18
3.1.2	Package Stack	5	4.3	Device Preparation	18
3.1.3	Package-on-Package (PoP)	5	4.3.1	Cleaning	18
3.1.4	Interposer	5	4.3.2	Baking	19
3.1.5	Through-Silicon Via (TSV)	6	4.3.3	Changing Termination Material	19
3.1.6	Through-Glass Via (TGV)	6	4.3.3.1	Deballing	19
3.1.7	System on Chip (SoC)	6	4.3.3.2	Reballing	19
3.1.8	System in Package (SiP)	6	4.3.3.3	Outsourcing Solutions	20
3.1.9	Wafer-Level Packaging (WLP)	6	4.3.3.4	Mixed/Backward Compatibility Solder Processing	20
3.1.10	Flip-Out Wafer-Level Packaging (FOWLP)	7	4.3.3.5	Underfill for Mixed-Alloy Soldering	20
3.1.11	Substrate	7	4.4	Passive-Component Integration (Organic Base Material)	21
3.2	Package Geometric Space	7	4.4.1	Formed Resistors	21
3.2.1	Two-Dimensional (2D) Package	7	4.4.1.1	Etch-Formed Resistors	21
3.2.2	Two-and-a-Half-Dimensional (2.5D) Package	8			
3.2.3	Three-Dimensional (3D) Package	8			

4.4.1.2	Discrete Resistors	21	5.8	Conductor Characteristics (Metallization on Ceramic)	33
4.4.2	Formed Capacitors	21			
4.4.2.1	Discrete (Placed) Capacitors	21	6	PROCESS MATERIALS	33
4.4.3	Formed Inductors	21	6.1	Adhesives (Conductive and Nonconductive)	33
4.4.4	Discrete Inductors	22	6.1.1	Polymer Adhesives	33
4.5	Passive Component Integration (Nonorganic Base Material)	22	6.1.1.1	Thermoset Materials	34
4.5.1	Formed Resistors	22	6.1.1.2	Thermoplastic Materials	34
4.5.2	Formed Capacitors	22	6.1.2	Dry-Film Adhesive	34
4.5.3	Formed Inductors	23	6.1.2.1	Die-Attach Film Application	34
4.6	Semiconductor Die Issues	23	6.2	Solder Materials	35
4.6.1	Surface Redistribution	23	7	PACKAGE-LEVEL STANDARDIZATION	35
4.7	Postprocess Validations	24	7.1	Package Outline Standards	35
4.7.1	Solder on Pad (Flip-Chip)	24	7.1.1	Ball Grid Array (BGA)	35
4.7.2	Known Good Die (KGD)	24	7.1.2	Fine-Pitch BGA (FBGA/FLBGA)	36
4.8	Component Handling	24	7.1.3	Package-on-Package (PoP)	37
4.8.1	Packaging	25	7.1.4	Through-Mold Via (TMV) Package-on-Package (PoP)	38
4.8.2	Component Storage	25	7.1.5	Wafer-Level Ball Grid Array (WLBGA)	38
4.9	Thermal Management of 3D Components	25	7.1.6	Stacked Chip Packaging Standards	38
4.9.1	Thermal Conduction/Convection	25	8	PRINTED BOARD AND OTHER MOUNTING BASE ON BOARD STACK-UP CONSIDERATIONS	39
4.9.2	Thermal Transfer Mechanisms	26	8.1	Printed Board Technology	39
4.9.3	Advanced Thermal Interface Materials	26	8.1.1	Multilevel Substrate	39
4.9.4	High-Conductivity Mold Compounds	28	8.2	Mounting Base	40
4.9.5	Liquid Cooling	28	8.3	Surface Finish for Placed Components	40
4.9.6	Microfluidic Cooling	29	8.3.1	Electroless Nickel/Immersion Gold (ENIG)	40
4.9.7	Single-Phase Intertier Cooling	29	8.3.2	Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)	40
4.9.8	Two-Phase Intertier Cooling	29	8.3.3	Organic Solderability Preservative (OSP)	40
4.9.9	Heat Pipes	29	8.3.4	Electrolytic Nickel/Electrolytic Gold (ENEG)	40
4.9.10	Microchannel and Minichannel Cooling	29	8.3.5	Direct Immersion Gold (DIG)	40
4.9.11	Thermal Modeling	30	8.3.6	Immersion Silver	40
4.10	Cost Consideration	30	8.3.7	Immersion Tin	41
5	INTERPOSER/SUBSTRATE MATERIALS	30	8.3.8	Cu (Chemical Deposition and Electroplate)	41
5.1	Organic Interposer	31	8.4	Embedded-Component Technology	41
5.1.1	Organic, CTE Matching Interposer Material	31	8.4.1	Formed Resistor Process	41
5.1.2	Organic-Based Interposer Fabrication Process	31	8.4.1.1	Design Criteria for Sheet-Film-Type Resistor Elements	42
5.2	Glass Interposer	31	8.4.2	Capacitor Formation Process	42
5.3	Silicon Interposers	31	8.4.3	Planar Capacitance	42
5.4	Ceramic Substrate/Interposer	32	8.4.3.1	Plane Layer Separation	42
5.5	Conductor Characteristics (Cu Foil/Film)	32	8.4.4	Discrete Formed Capacitor Element	42
5.6	Conductor Characteristics (Metallization on Silicon)	32			
5.7	Conductor Characteristics (Metallization on Glass)	33			

8.4.5	Discrete Inductor Forming	42	9.2.1.2	Ceramic-Based Interposer Design	50
8.4.6	Discrete Component Placement	43	9.2.2	External (Surface) Component Mounting	50
8.4.6.1	Discrete Resistor and Capacitor Placement	43	9.2.2.1	Solder Attachment	50
8.4.6.2	Discrete Inductor Placement	43	9.2.2.2	Conductive Polymer Attachment	50
8.4.6.3	Active-Die Element Placement	43	9.2.3	Internal (Embedded) Component Mounting	50
8.4.6.4	Surface Finishes for UBM Plating	44	9.2.4	Circuit Interface Techniques	50
8.4.6.4.1	Electroless Nickel/Immersion Gold (ENIG)	44	9.2.4.1	Organic-Based Interposer Design	50
8.4.6.4.2	Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG)	44	9.2.5	Internal Discrete Heat Sink	50
8.4.6.4.3	Cu Under-Bump Metallization (UBM) Plating	44	9.2.5.1	Organic-Based Interposer Design	52
8.4.6.5	Redistribution Layer (RDL) Process	44	9.3	Layout Strategy	52
8.5	Substrate and Interposer Materials (Package Level)	44	9.3.1	Product Functional Description	52
8.5.1	Organic Circuit Structure	45	9.3.2	Engineering Actions	52
8.5.2	Ceramic Circuit Structure	45	9.3.3	Design Density Analysis	52
8.5.2.1	Metallization on Ceramic	45	9.3.4	Embedded Component Selection	53
8.5.3	Silicon Circuit Structure	45	9.3.4.1	Embedding Passive Components	53
8.5.4	Glass Circuit Structure	45	9.3.4.2	Embedding Active Components	53
8.6	Dielectric Impregnation	46	9.3.5	Embedded Component Circuit Interface	53
8.6.1	Reinforced Prepreg	46	9.4	Multilayer Substrate Construction and Geometries	54
8.6.2	Unreinforced Resin	46	9.4.1	Build-Up Circuit Layers on Glass Base Structures	54
8.6.3	Resin-Coated Cu (RCC)	46	9.4.2	Build-Up Circuit Layers on Silicon Base Structures	54
8.7	Via Hole Preparation and Interconnectivity	46	9.5	Component Attachment on Multilevel Assembly	55
8.7.1	Through-Glass Via (TGV) Connection to Printed Board Cu	46	9.5.1	Conductive Polymers	55
8.7.2	Through-Glass Via (TGV) Connection to Component Termination	46	9.5.2	Dry-Film Adhesives	55
8.7.3	Through-Glass Via (TGV) Formation	46	9.5.3	Solder Attachment	55
8.7.4	Through-Silicon Via (TSV) Formation	47	9.6	Circuit Routing Strategy (Organic and Nonorganic)	55
8.7.5	Via Filling	47	9.6.1	Organic-Based Substrates	55
8.7.6	Alternative Via Plating on Silicon-Based Interposer	47	9.6.2	Silicon and Glass Interposers	55
8.7.7	Conductor Forming on Silicon Interposers	48	9.6.3	Ceramic-Based Substrates and Interposers	55
8.8	Build-Up Layers and Via Hole Preparation – Redistribution Layer (RDL) on Silicon and Glass	48	9.7	Documentation	55
8.8.1	Silicon Interposer Metallization	48	9.7.1	Documentation Package	56
8.8.2	Glass Interposer Metallization	48	9.7.2	Bill of Materials (BoM)	56
8.9	Multilevel Printed Board – Cavity Board	48	9.7.3	Software Tools and Data Transfer	56
9	DESIGN METHODOLOGY	49	9.7.4	General Rules for 3D Design	56
9.1	Design Challenges	49	10	ASSEMBLY OF 3D PACKAGES ON PRINTED BOARDS	56
9.2	Total Circuit Consideration	49	10.1	Package-on-Package (PoP) Assembly Process	56
9.2.1	Internal (Embedded) Component Mounting	49	10.1.1	Package-on-Package (PoP) Fluxing Options	57
9.2.1.1	Organic-Based Interposers	49	10.1.2	Package-on-Package (PoP) Fluxing Process	57
			10.1.2.1	Flux Coverage	58

10.1.2.2	Dwell Time (Hold Time) Speed	58	10.9.3	Removable and Reworkable Underfill	71
10.1.2.3	Retracting Speed	58	10.9.4	Corner Bonding/Glue Bonding	71
10.1.2.4	Retracting Force	58	10.9.5	Molded Underfill (MUF)	71
10.1.3	Flux Height Statistical Process Control	58	10.9.6	Vacuum Underfill (VUF)	72
10.1.4	Paste Dip	59	10.9.7	Wafer-Applied Underfill	72
10.1.5	Prestacking Process	59	10.9.8	Underfill Inspection	72
10.1.6	Through-Mold Via (TMV) Assembly Considerations	59	10.9.8.1	Causes of Voids	72
10.1.7	Package-on-Package (PoP) Stand-Off Height (SOH)	60	10.9.8.2	Void Characteristics	73
10.1.8	Package-on-Package (PoP) Die Gap	60	10.9.8.3	Test Strategies	73
10.2	Three-Dimensional (3D) Printing	61	10.9.8.4	Flow-Pattern Voids	73
10.2.1	Cavity Printing	61	10.9.8.5	Moisture Voids	73
10.2.2	Jet Printing	61	10.9.8.6	Effect of Contamination	73
10.2.3	Paste Dispensing	61	11 TESTING AND PRODUCT VERIFICATION		73
10.2.4	Cavity Keep-Out Zone	62	11.1	Establishing Test Requirements	73
10.3	Multilevel Placement	62	11.2	Assembly Process Qualification	74
10.3.1	Parameters	62	11.2.1	Package-Level Stress Tests	74
10.3.2	Cavity Design	64	11.3	Substrate Test Coupons	75
10.3.3	Plateau Design	64	12 RELIABILITY		75
10.4	Die Attachment	64	12.1	Reliability Considerations	75
10.4.1	Direct Chip Attachment	64	12.2	Design for Reliability (DfR) Principles	76
10.4.2	Die-to-Substrate Reinforcement	64	12.3	End-Use Relationship	77
10.5	Reflow Soldering Considerations for 3D Components	65	12.3.1	Temperature Cycle Condition	77
10.5.1	Low-Temperature Soldering (LTS) of 3D Components	65	12.3.2	Test Duration	77
10.5.1.1	Drivers for Low-Temperature Solders in 3D Assembly	65	12.3.3	Number of Samples	77
10.5.1.2	Choice of Low-Temperature Solder Alloys	66	12.4	Effects of Pb-Free Materials and Pure-Sn Finishes on Reliability	78
10.5.1.3	Mixed-Alloy LTS-SAC (Hybrid Solder)	67	12.5	Validation, Qualification and Accelerated Aging Test for Reliability	78
10.6	3D Component Inspection Techniques	67	12.6	Environmental Testing	78
10.6.1	X-Ray Inspection Techniques	67	13 DEFECT AND FAILURE ANALYSIS		79
10.6.2	Acoustic Microscopy (AM) Inspection Techniques	68	13.1	Nondestructive Failure Analysis	79
10.7	Board-Level Rework	68	13.1.1	Electrical Testing	79
10.7.1	Rework with Convection Reflow Soldering	70	13.1.1.1	Functional Testing (FT)	79
10.7.2	Rework with Infrared (IR) Reflow Soldering	70	13.1.1.2	Modeled Fault Testing (MFT)	79
10.7.3	Rework with Laser Soldering	70	13.1.1.3	Iddq	79
10.8	Underfill	71	13.1.1.4	Time-Domain Reflectometer (TDR)	79
10.9	Package-to-Printed Board Reinforcement	71	13.2	Internal Nondestructive Inspection	79
10.9.1	Material Selection and Application	71	13.2.1	Acoustic Microscopy (AM)	80
10.9.2	Capillary Flow Underfill	71	13.2.2	X-Ray Imaging	80
10.9.3	No-Flow/Fluxing Underfill	71	13.2.3	Infrared (IR)	80
			13.2.3.1	Infrared (IR) Thermography (IRT)/Thermal Imaging	80

13.2.3.2	Infrared (IR) Microscopy	80	Figure 3-8	Example of a 2.5D System in Package (SiP)	8
13.2.4	Magnetic Current Imaging (MCI)	81	Figure 3-9	3D Package-on-Package (PoP) and System in Package (SiP) on a Printed Board.	8
13.2.5	Internal Optical Inspection	81	Figure 3-10	Ball Grid Array (BGA) Substrate with Embedded Active and Passive Elements	9
13.2.6	Electrical Probing/Nanoprobing	81	Figure 3-11	Advanced Package Trends	9
13.2.7	Chemical Analysis	81	Figure 4-1	Comparing Current Two-Die and Quad-Die Package Solutions	10
13.3	Destructive Failure Analysis	81	Figure 4-2	Standard Package-on-Package (PoP) Example with Stacked Die	11
13.3.1	Cross-Sectioning	81	Figure 4-3	Through-Mold Via (TMV) Package-on-Package (PoP)	11
13.3.2	Parallel Lapping	82	Figure 4-4	Lower Package-on-Package (PoP) Section with Through-Mold Vias (TMVs)	11
13.3.3	Decapsulation	82	Figure 4-5	Through-Mold Via (TMV) Solder Balls	11
13.4	Optical Inspection	82	Figure 4-6	Lower Package-on-Package (PoP) Section with Through Mold Interconnect (TMI)	12
13.4.1	Optical Inspection (After Assembly)	82	Figure 4-7	Cu Pillar Interconnect (CuPI) Package-on-Package (PoP)	13
13.4.2	Confocal Laser Scanning Microscopy (CLSM)	83	Figure 4-8	High-Density Micro-Pillar (μ PILR) Array Packaging	13
13.5	Examples of Observed External Inspection Defects	83	Figure 4-9	Bond Via Array (BVA) With Fine-Pitch Cu Wire Interconnect	13
13.5.1	Head on Pillow (HoP) Defect	83	Figure 4-10	Direct Bond Interface (DBI)	14
13.5.2	Package-on-Package (PoP) Joining Defects	83	Figure 4-11	Three-Memory Die on Flexible Circuit Substrate	14
13.5.3	Nonwet Open (NWO) Joint	83	Figure 4-12	Package-on-Package Interposer (PoPi)	14
13.5.4	Bridging on Package-on-Package (PoP)	83	Figure 4-13	Stacked Thin Small Outline Package (TSOP) Devices	15
13.5.5	Through-Mold Via Head on Pillow (HoP)	83	Figure 4-14	High-Band Memory (HBM)	15
13.5.6	Insufficient Solder/Flux	84	Figure 4-15	Silicon Bridge Interposer with Stacked Die and HBM	15
13.5.7	Incomplete Solder Reflow	84	Figure 4-16	Embedded Multi-Die Interconnect Bridge (EMIB)	16
13.5.8	Missing Solder Ball	84	Figure 4-17	Through-Silicon Via (TSV)	16
13.5.9	Nonuniform or Missing Solder Deposition	84	Figure 4-18	Fusion Bond Process	17
13.5.10	Voids and Uneven Solder	85	Figure 4-19	Intermetallic Bonds (Cu/Cu ₃ Sn/Cu)	17
14	SUBASSEMBLY CONTRACTOR SELECTION AND QUALIFICATION	85	Figure 4-20	Intermetallic Thermo-compression Bonding	18
14.1	Factory and Process Audits	85	Figure 4-21	Benchtop Small-Batch Ultrasonic Cleaner	18
14.2	Site Visit Procedure	85	Figure 4-22	JEDEC-Compliant Carrier Tray	19
14.3	Design and Process Evaluation	85	Figure 4-23	SnPb and Mixed-Metallurgy Ball Grid Array (BGA) Solder Joints	20
14.4	Observations and Recommendations	86	Figure 4-24	Formed Resistor Elements	21
Appendix A	Abbreviations and Acronyms	87	Figure 4-25	Trench or Pillar Capacitor in Silicon	22
	Figures				
Figure 1-1	3D Technology Complexity	2			
Figure 3-1	Die Stack Package Assembly	5			
Figure 3-2	Mixed-Function Package-on-Package (PoP) Example	5			
Figure 3-3	System on Chip (SoC) Example	6			
Figure 3-4	System in Package (SiP) Example	6			
Figure 3-5	Wafer-Level Packaging (WLP) for High-Performance Memory	6			
Figure 3-6	Fanout Wafer Level Package Examples	7			
Figure 3-7	Example of a 2D System in Package	7			

Figure 4-26	Surface Redistribution	23	Figure 8-3	Pull-Up and Pull-Down Resistors Using Thin-Film Material	41
Figure 4-27	Contact Variations for Flip-Chip Mounting.	24	Figure 8-4	Formed Multilayer Capacitor Element.	42
Figure 4-28	Partitioned Carrier Trays for Ball Grid Array (BGA) Components	25	Figure 8-5	Etched Cu Spiral Inductor Pattern	43
Figure 4-29	Tape-and-Reel Format	25	Figure 8-6	0603 Components Embedded into a Cavity Feature in the Substrate.	43
Figure 4-30	Thermal Conduction.	26	Figure 8-7	Three-Dimensional (3D) Die Stack Package Using Cu Wire-Bond Processing	44
Figure 4-31	Thermal Transfer Paths.	26	Figure 8-8	Additive Redistribution Layer (RDL) to Array Contact Site	44
Figure 4-32	Thermal Resistance Versus Bondline Thickness for State-of-the-Art Thermal Greases and Gels.	27	Figure 8-9	Merging Organic and Silicon-Based Materials for 3D Semiconductor Packaging	45
Figure 4-33	Advances in Thermal Resistance with Thinner and Higher-Conductivity Reliable Materials.	27	Figure 8-10	Ceramic-Based Interposer	45
Figure 4-34	Nanosilver Interconnections.	27	Figure 8-11	Through-Glass Via (TGV)	46
Figure 4-35	Advances in 3D Packages with Fan-Out Wafer-Level Packaging (FOWLP) and Die-Embedding (Left) and High-Thermal-Conductivity Composites with Advanced Boron Nitride Fillers and Surface Treatments (Right).	28	Figure 8-12	Through-Glass Via (TGV)-Formed Glass Substrates	46
Figure 4-36	Liquid Heat Pipe Exchange System	28	Figure 8-13	Metallized Through-Glass Via (TGV) X-Ray Photos	47
Figure 4-37	Comparison of 3D Integrated Circuits (ICs) Utilizing Different Cooling Technologies	29	Figure 8-14	Cu-Filled Through-Silicon Via (TSV) Interface Between Wafers – Active Side and Back Side	47
Figure 5-1	Simulated Insertion Loss (S_{21}) of Through-Glass Via (TGV) and Through-Silicon Via (TSV) Interconnects.	31	Figure 8-15	Comparing Via Deposition Methodology.	48
Figure 5-2	Glass Wafer and Panel Substrates.	31	Figure 8-16	Comparison of Component in a Cavity Versus on the Board Surface.	48
Figure 5-3	Microcrystalline-Silicon Ingot	32	Figure 8-17	Cavity Design Example	49
Figure 5-4	Flattened Feature on Wafer Edge Identifies Wafer Orientation During Fabrication Processes.	32	Figure 9-1	Embedded Semiconductor Substrate	54
Figure 5-5	Ceramic Panel Prior to Metallization	32	Figure 9-2	Glass Interposer With 40- μm Pitch Bumps and $L/S = 2 \mu\text{m} / 2 \mu\text{m}$	54
Figure 7-1	Ball Grid Array (BGA) Package Outline	36	Figure 9-3	Two-Layer Build-Up Circuit Interposer	54
Figure 7-2	Fine-Pitch Ball Grid Array (FBGA/FIBGA)	36	Figure 10-1	Package-on-Package (PoP) Assembly Principle	57
Figure 7-3	Fine-Pitch Ball Grid Array (FBGA/FIBGA) Contact Diameter and Pitch Variations.	37	Figure 10-2	Package-on-Package (PoP) Fluxing Units	57
Figure 7-4	JEDEC Package-on-Package (PoP) Construction Variations.	37	Figure 10-3	Ball Grid Array (BGA) Flux Coverage	58
Figure 7-5	Contact Redistribution at the Wafer Level Provides a Method for Furnishing a Uniform Array Format to Better Accommodate Face-Down Mounting.	38	Figure 10-4	Flux Transfer to a Cu Coupon	58
Figure 8-1	Two-Level Substrate with Embedded Components	39	Figure 10-5	Flux Height Measurement Gauges	58
Figure 8-2	Ball Grid Array (BGA) Package Adopting an Embedded-Component Substrate.	41	Figure 10-6	Solder Balls After Paste Dip.	59
			Figure 10-7	Carrier with Prestacked Packages.	59
			Figure 10-8	Soldering Surface of Through-Mold Via (TMV) Balls	59
			Figure 10-9	Ball Collapse.	59
			Figure 10-10	Z-Height of a Package-on-Package (PoP)	60
			Figure 10-11	Joint Stand-Off Height (SOH)	60
			Figure 10-12	Package-on-Package (PoP) Die Gap	60

Figure 10-13	Cavity and 3D Stencil	61	Figure 10-38	Comparing Two-Step Underfill Plus Mold Process (A) to the One-Step Molded Underfill Packaged Die (B)	72
Figure 10-14	Three-Dimensional (3D) Stencil with a Cavity Pocket on the Right	61	Figure 10-39	Void in Underfill Under Array-Configured Flip-Chip Die	72
Figure 10-15	Slit-Metal Squeegee	61	Figure 11-1	Quality Document System	75
Figure 10-16	Package-on-Package (PoP) Mounted into a Cavity	61	Figure 13-1	Acoustical Microscopy (AM) Can Identify Voids, Delamination and Cracks	80
Figure 10-17	Jet Printing of Solder Paste for a 0.8-mm [0.031-in] BGA	61	Figure 13-2	3D Submicron X-Ray Imaging Distinctly Identifying Solder Bridging	80
Figure 10-18	Multiple-Deposit Jet Printing for Customized Deposit Volumes	62	Figure 13-3	Die-to-Silicon-to-Substrate Assembly	82
Figure 10-19	3D Jet Printing on Camera Module	62	Figure 13-4	Semiconductor Package Decapsulation System	82
Figure 10-20	Cavity Keep-Out Zone	62	Figure 13-5	Head on Pillow (HoP) Solder Process Defect	83
Figure 10-21	Multilevel Printed Board	62	Figure 13-6	Poor Coalesce Between Sphere and Interposer Land	83
Figure 10-22	Avoiding Interference in Multilevel Placement Design	63	Figure 13-7	Nonwetting Defect, Exhibiting the Effect of Excessive Oxidation	83
Figure 10-23	Principle of Fiducial Hierarchy and Placement Precedence	63	Figure 13-8	Endoscopy Edge View of Solder Bridge Between Ball Grid Array (BGA) Sphere Contacts	83
Figure 10-24	Capillary Flow of Liquid Epoxy Fully Encapsulating and Stabilizing the Area Between Two Parallel Surfaces	64	Figure 13-9	Bridging on Package-on-Package (Pop)	84
Figure 10-25	Soldering Material in Package-on-Package (PoP) Assembly	65	Figure 13-10	Defect Attributed to Oxide Contamination	84
Figure 10-26	SiP and PoP Assembly	65	Figure 13-11	Comparison of Wetting Characteristics of Two Surface Finishes	84
Figure 10-27	Board Stacking with Interposer	66	Figure 13-12	Incomplete Solder Reflow	84
Figure 10-28	Low-Temperature Alloys with Liquidus Temperatures Between 100 °C and 200 °C and Which Do Not Contain Pb, Cd or Au	66	Figure 13-13	Missing Solder Ball	84
Figure 10-29	Mixed-Alloy BGA Solder Joint Formed with SAC Ball Soldered with Ductile Metallurgy BiSn Solder Paste	66	Tables		
Figure 10-30	Package-on-Package (PoP) With Overlapping Memory Balls	67	Table 4-1	Through-Mold Via (TMV) Examples	12
Figure 10-31	Package-on-Package (PoP) with Overlapping Memory Balls Viewed with 3D Laminography X-Ray	67	Table 5-1	Interposer Material Properties Comparison	30
Figure 10-32	Head on Pillow (HoP) 3D Laminography Image	68	Table 7-1	Plastic Ball Grid Array (PBGA) Contact Diameter and Pitch Variations	36
Figure 10-33	Tilted 2D X-Ray View of Through-Mold Interconnect (TMI) Package-on-Package (PoP) with Head on Pillow (HoP) Defect on the Memory	68	Table 7-2	Fine-Pitch Ball Grid Array (FBGA/FIBGA) Contact Diameter and Pitch Variations	37
Figure 10-34	AM Images of a 3D Devices with and without Acceptable Defects	69	Table 7-3	Comparing Wafer-Level Ball Grid Array (WLBGA) Contact Pitch to Ball or Bump Contact Diameter Range	38
Figure 10-35	Rework with Laser Soldering	70	Table 9-1	Typical Feature Sizes for High Density Interconnect (HDI) Substrate Constructions, μm [mil]	51
Figure 10-36	Package-to-Printed Board Reinforcement	70	Table 10-1	Stand-Off Height (SOH) of 0.4-mm [0.016-in] Package-on-Package (PoP) With 200- μm Balls	60
Figure 10-37	Edge Dispensing of Underfill Material	71			

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Design and Assembly Process Implementation of 3D Components

1 SCOPE

This document describes the design and assembly challenges and ways to address those challenges for implementing 3D component technology. Recognizing the effects of combining multiple uncased semiconductor die elements in a single-package format can impact individual component characteristics and can dictate suitable assembly methodology. The information contained in this standard focuses on achieving optimum functionality, process assessment, end-product reliability and repair issues associated with 3D semiconductor package assembly and processing.

1.1 Purpose Performance-driven electronic systems continue to challenge companies in search of more innovative semiconductor package methodologies. The key market driver for semiconductor package technology is to provide greater functionality and improved performance without increasing package size. The package interposer is the key enabler. Although glass-reinforced epoxy-based materials and high-density Cu interconnect capability will continue to have a primary role for array-configured packaging, there is a trend toward alternative dielectric platforms as well as toward combining multiple functions within the same die element. To address this movement, an increasing number of semiconductor die developed for advanced applications now require higher I/O with contact pitch variations that are significantly smaller than the mainstream semiconductor products previously in the market. For these applications, companies are developing interposer technologies that can provide interconnect densities far superior to organic-based counterparts.

1.1.1 Target Audience The target audiences for this standard are managers, design/process engineers and operators who deal with:

- Implementing 3D semiconductor packaging
- Interposer, substrate and printed board design
- Board-level assembly, inspection and repair processes

1.1.2 Intent This standard intends to provide useful and practical information to those who are designing, developing or using 3D-packaged semiconductor components or those who are considering 3D package implementation. The 3D semiconductor package may include multiple die elements—some homogeneous and some heterogeneous. The package may also include several discrete passive SMT devices, some of which are surface mounted and some of which are integrated (embedded) within the components' substrate structure.

1.2 Classification IPC standards recognize that electrical and electronic assemblies are subject to classifications by intended end-item use. Three general end-product classes have been established to reflect differences in manufacturability, complexity, functional performance requirements, and verification (inspection/test) frequency. It should be recognized that there may be overlaps of equipment between classes.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically, the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

1.3 Measurement Units All dimensions and tolerances in this specification are expressed in hard SI (metric) units and bracketed soft imperial [inch] units. Users of this specification are expected to use metric dimensions. All dimensions ≥ 1 mm [0.0394 in] will be expressed in millimeters and inches. All dimensions < 1 mm [0.0394 in] will be expressed in micrometers and microinches.

1.4 Use of "Lead" For readability and translation, this document uses the noun lead only to describe leads of a component. The metallic element lead is always written as Pb.

1.5 Abbreviations and Acronyms Periodic table elements are abbreviated in the standard. See Appendix A for full spellings of abbreviations (including elements) and acronyms used in this standard.