

IPC/JPCA-2291

2013 - June

Design Guideline for Printed Electronics

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Association Connecting Electronics Industries



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Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

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IPC/JPCA-2291

JPCA

Design Guideline for Printed Electronics



Developed by the Printed Electronics Design Subcommittee (D-61) of the
Printed Electronics Committee (D-60) of IPC

Users of this publication are encouraged to participate in the
development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105

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Acknowledgment

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Printed Electronics Committee

Chair
Daniel Gamota
Jabil Circuit, Inc.

Printed Electronics Design Subcommittee

Co-Chairs
Daniel Gamota
Jabil Circuit, Inc.

Jie Zhang
Institute of Materials
Research & Engineering (IMRE)

JPCA Printed Electronics Committee

Chair
Dr. Prof. Katsuaki Suga
Osaka University, Institute of
Scientific and Industrial Research

Technical Liaison of the IPC Board of Directors

Bob Neves
Microtek (Changzhou) Laboratories

Printed Electronics Design Subcommittee

John Andresakis, Oak-Mitsui, Inc.
Neil Bolding, MacDermid Autotype Inc
Robert Boudreau, Corning Incorporated
Luis Chau, MFLEX
Christine Coapman, C2 Consulting
Daniel Gamota, Jabil Circuit, Inc. (HQ)
Mahendra Gandhi, Northrop Grumman Aerospace Systems
Josh Goldberg, Taiyo America Inc
Tom Hartmann, Topflight Corporation
Happy Holden, Gentex Corporation
Hirofumi Matsumoto, Nippon Mektron Ltd.

Stephen Meeks, St. Jude Medical
Roger Miedico, Raytheon Company
Richard Morris, Saxby Business Development LLC
Steve Nolan, Lockheed Martin Mission Systems & Training
Debbie O'Connell, PLES
Cary Scarffler, Lockheed Martin Missile & Fire Control
Dingkai Shangguan, National Center for Advanced Packaging, China
Masato Shishido, JPCA-Japan Electronics Packaging and Circuits Association
Jeffrey Shubrooks, Raytheon Company

David Sommervold, The Bergquist Company, Prescott
Katsuaki Suga, Osaka University
Kunio Takahara, JPCA-Japan Electronics Packaging and Circuits Association
Diane Williams, Corning Incorporated
Yukihiro Yoshida, Mitsubishi Plastics, Inc.
Jie Zhang, Institute of Materials Research & Engineering (IMRE)

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DESIGN GUIDELINES FOR PRINTED ELECTRONICS

1 SCOPE

This guideline provides an overview of the design process flow for printed electronics based devices, modules and units, and final products.

1.1 Purpose The purpose is to present the framework of the design process flow for individuals to manufacture printed electronics based devices, modules and units, and final products.

1.2 Intent The intent of IPC/JPCA-2291 is to establish a design process flow that will facilitate and improve the practice of printed electronics design. IPC/JPCA-2291 identifies documents such as standards that can be used to assist during the design process flow. In general IPC/JPCA-2291 contains generic information that is sufficient for printed electronics design by the product designer.

The subcommittee members that developed IPC/JPCA-2291 acknowledge that individual companies may require additional information than that reported within this document. Therefore, IPC/JPCA-2291 and documents specified within it may only reflect a subset of those required by members of the supply chain.

IPC/JPCA-2291 is “generic” because it specifies only information which forms the basis for further specific declarations. It is therefore intended to be used in conjunction with other documents as needed. Also part of the intent is to provide mechanisms for securing the integrity of the information exchanged between supply chain members.

1.3 Printed Electronics Document Hierarchy The IPC/JPCA printed electronics standards development subcommittees have established a hierarchy as presented in Figure 1-1 based on the existing initiatives. It was structured to enable the greatest flexibility for the emerging field of printed electronics. The subcommittees plan to revisit it frequently and modify it as necessary during the growth of the field and technologies transition from R&D to commercialization.

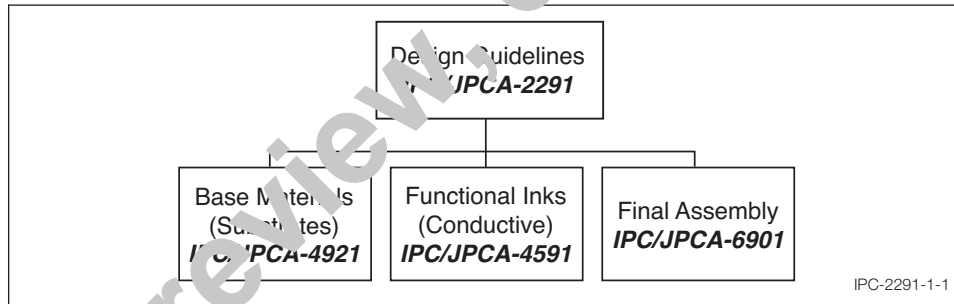


Figure 1-1 Hierarchy for IPC/JPCA Printed Electronics Documents

As the documents listed in Figure 1-1 are completed, new standards projects may be undertaken by the subcommittees. Proposed projects will be listed as shown in Figure 1-2; a project was proposed that addresses manufacturing processes and platforms. In addition to initiating new project topics, subcommittees may also be actively preparing a revision of a previously approved standard based on recent subcommittee member comments as well as general industry trends.

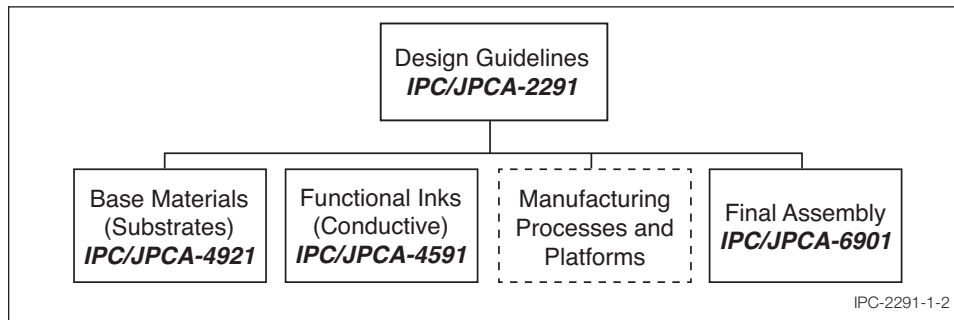


Figure 1-2 Future Hierarchy for IPC/JPCA Printed Electronics Documents