

IPC-2221B

2012 - November

Generic Standard on Printed Board Design

Supersedes IPC-2221
May 2003

A standard developed by IPC

Association Connecting Electronics Industries



The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee (TAEC) adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to Design for Manufacturability (DFM) and Design for the Environment (DFE)
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are and are wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

IPC Position Statement on Specification Revision Change

It is the position of IPC's Technical Activities Executive Committee that the use and implementation of IPC publications is voluntary and a part of a relationship entered into by customer and supplier. When an IPC publication is updated and a new revision is published, it is the opinion of the TAEC that the use of the new revision as part of an existing relationship is not automatic unless required by the contract. The TAEC recommends the use of the latest revision. Adopted October 6, 1998

Why is there a charge for this document?

Your purchase of this document contributes to the ongoing development of new and updated industry standards and publications. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards and publications development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low to allow as many companies as possible to participate. Therefore, the standards and publications revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards and publications, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/597-2872.

Thank you for your continued support.



IPC-2221B

Generic Standard on Printed Board Design

Developed by the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) of IPC

Supersedes:

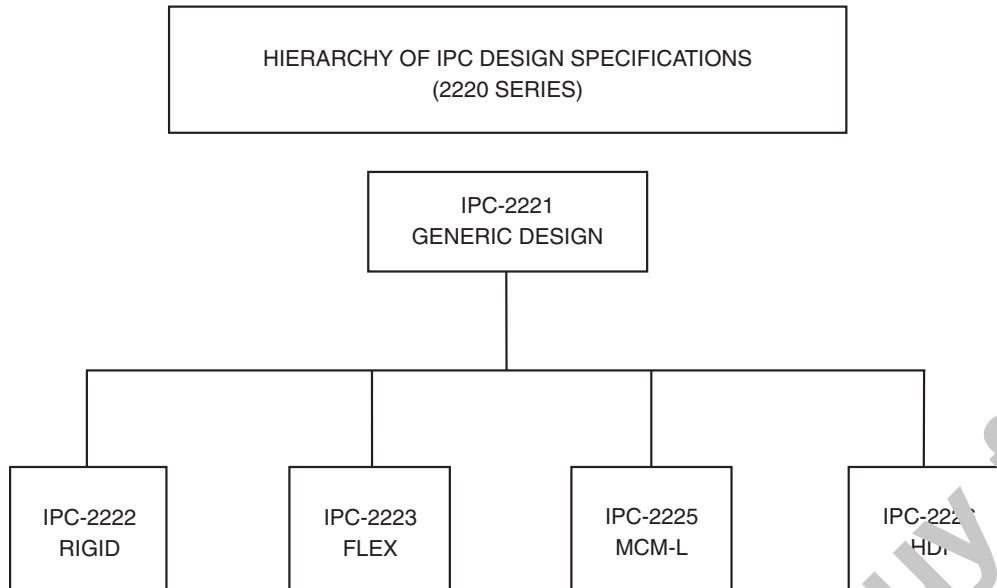
IPC-2221A - May 2003

IPC-2221 - February 1998

Users of this publication are encouraged to participate in the development of future revisions.

Contact:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, Illinois
60015-1249
Tel 847 615.7100
Fax 847 615.7105



FOREWORD

This standard is intended to provide information on the generic requirements for organic printed board design. All aspects and details of the design requirements are addressed to the extent that they can be applied to the broad spectrum of those designs that use organic materials or organic materials in combination with inorganic materials (metal, glass, ceramic, etc.) to provide the structure for mounting and interconnecting electronic, electromechanical, and mechanical components. It is crucial that a decision pertaining to the choice of product types be made as early as possible. Once a component mounting and interconnecting technology has been selected the user should obtain the sectional document that provides the specific focus on the chosen technology.

It may be more effective to consider alternative printed board construction types for the product being designed. As an example the application of a rigid-flex printed wiring board may be more cost or performance effective than using multiple printed wiring boards, connectors and cables.

IPC's documentation strategy is to provide distinct documents that focus on specific aspect of electronic packaging issues. In this regard document sets are used to provide the total information related to a particular electronic packaging topic. A document set is identified by a four digit number that ends in zero (0).

Included in the set is the generic information which is contained in the first document of the set and identified by the four digit set number. The generic standard is supplemented by one or many sectional documents each of which provide specific focus on one aspect of the topic or the technology selected. The user needs, as a minimum, the generic design document, the sectional of the chosen technology, and the engineering description of the final product.

As technology changes specific focus standards will be updated, or new focus standards added to the document set. The IPC invites input on the effectiveness of the documentation and encourages user response through completion of "Suggestions for Improvement" forms located at the end of each document.

Acknowledgment

Any document involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-2221 Task Group (D-31b) of the Rigid Printed Board Committee (D-30) are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

Rigid Printed Board Committee	IPC-2221/2222 Task Group	Technical Liaison of the IPC Board of Directors
Chair Vicka White Honeywell Aerospace	Chair Gary Ferrari FTG Circuits	Dongkai Shangguan Flextronics International
Vice-Chair Debora Obitz Trace-Laboratories - Baltimore	Vice-Chair Cliff Maddox Boeing Company	Shane Whiteside TTM Technologies
IPC-2221 Task Group		
Alisha A. Amar, Lockheed Martin Space Systems Company	Mark Finstad, Flexible Circuit Technologies, Inc.	Debora L. Obitz, Trace Laboratories - Baltimore
Lance A. Auer, Raytheon Missile Systems	Larry F. Foster, Lockheed Martin Missiles & Fire Control	Gerard O'Brien, Solderability Testing & Solutions, Inc.
Robert F. Bagsby, Rockwell Collins	Lionel Fullwood, WKK Distribution Ltd.	Jack C. Olson, Caterpillar Inc.
John A. Bauer, Rockwell Collins	Mahendra S. Gandhi, Northrop Grumman Aerospace Systems	William A. Orloff, Raytheon Company
Wendi Boger, Viasystems Group, Inc.	Tom Gardenour, Amphenol Printed Circuits, Inc.	Stephen G. Pierce, SGP Ventures, Inc.
Gerald Leslie Bogert, Bechtel Plant Machinery, Inc.	Michael R. Green, Lockheed Martin Space Systems Company	Randy R. Reed, Viasystems Group, Inc.
Scott A. Bowles, L-3 Fuzing and Ordnance Systems	Philip M. Renault, Raytheon Company	Jose A. Rios, Endicott Interconnect Technologies Inc
Steven A. Bowles, Viasystems Group, Inc.	Joseph F. Kane, BAE Systems Platform Solutions	Joseph Schmidt, Raytheon Missile Systems
Mark Buechner, BAE Systems	Cliff Lewis, Holaday Circuits Inc.	Douglas R. Schueller, AbelConn, LLC
Byron Case, L-3 Communications	Anne Lomonte, Draeger Medical Systems, Inc.	Gilbert Shelby, Raytheon Systems Company
Calette Chamness, U.S. Army Aviation & Missile Command	Chris Mahanna, Robisan Laboratory Inc.	Robert Sheldon, Pioneer Circuits Inc.
Denise Chevalier, Amphenol Printed Circuits, Inc.	Kenneth J. Manning, Raytheon Company	Russell S. Shepherd, Microtek Laboratories
Christine Coapman, Delphi Electronics and Safety	Karen E. McConnell, Northrop Grumman Corporation	Lowell Sherman, Defense Supply Center Columbus
David J. Corbett, Defense Supply Center Columbus	Peter Menuiez, L-3 Communications - Cincinnati Electronics	Valerie A. St. Cyr, Teradyne Inc.
William C. Dieffenbacher, BAE Systems Platform Solutions	Roger J. Miedico, Raytheon Company	Bradley Toone, L-3 Communications
C. Lynn D. Priest, Lockheed Martin Missiles & Fire Control	George Milad, Uyemura International Corp.	Crystal E. Vanderpan, UL LLC
Patricia S. Dupuis, Raytheon Company	Michael P. Miller, NSWC Crane	Juan Vasquez, Viasystems Group, Inc.
Theodore Edwards, Dynaco Corp.	Steven M. Nolan, Lockheed Martin Maritime Systems & Sensors	Vicka White, Honeywell Aerospace
Timothy A. Estes, Conductor Analysis Technologies, Inc.		Dewey Whittaker, Honeywell Aerospace

This Page Intentionally Left Blank

Currently in preview, click buy full version

Table of Contents

1	SCOPE	1	4	MATERIALS	21
1.1	Purpose	1	4.1	Material Selection	21
1.2	Documentation Hierarchy	1	4.1.1	Material Selection for Structural Strength	21
1.3	Presentation	1	4.1.2	Material Selection for Electrical Properties	21
1.3.1	Dimensional Units	1	4.1.3	Material Selection for Environmental Properties	21
1.4	Interpretation	1	4.2	Dielectric Base Materials (Including Prepregs and Adhesives)	21
1.5	Definition of Terms	2	4.2.1	Preimpregnated Bonding Layer (Prepreg)	22
1.5.1	Microvia	2	4.2.2	Adhesives	22
1.6	Classification of Products	2	4.2.3	Adhesive Films or Sheets	24
1.6.1	Printed Board Type	2	4.2.4	Electrically Conductive Adhesives	24
1.6.2	Performance Classification	2	4.2.5	Thermally Conductive, Electrically Insulating Adhesives	24
1.6.3	Producibility Level	2	4.3	Laminate Materials	25
1.7	Revision Level Changes	3	4.3.1	High Temperature Laminates	25
2	APPLICABLE DOCUMENTS	3	4.3.2	Color Pigmentation	25
2.1	IPC	3	4.3.3	Dielectric Thickness/Spacing	25
2.2	Joint Industry Standards	4	4.3.4	Thermally Conductive Laminates	25
2.3	Society of Automotive Engineers	5	4.3.5	Minimum Base Material Thickness for PC Card Form Factors	26
2.4	American Society for Testing and Materials	5	4.4	Conductive Materials	26
2.5	Underwriters Labs	5	4.4.1	Electroless Copper Plating	29
2.6	IEEE	5	4.4.2	Semiconductive Coatings	29
2.7	ANSI	5	4.4.3	Electrolytic Copper Plating	29
2.8	ANSI/ESD	5	4.4.4	Gold Plating	29
2.9	PCMCIA	5	4.4.5	Immersion Silver	31
3	GENERAL REQUIREMENTS	6	4.4.6	Immersion Tin	31
3.1	Information Hierarchy	8	4.4.7	Organic Solderability Preservative (OSP)	32
3.1.1	Order of Precedence	8	4.4.8	Nickel Plating	32
3.1.2	End-Product Performance Requirements	8	4.4.9	Tin/Lead Plating	33
3.2	Design Considerations	8	4.4.10	Solder Coating	33
3.3	Schematic/Logic Diagram	9	4.4.11	Other Metallic Coatings for Edge Printed Board Contacts	34
3.4	Density Evaluation	9	4.4.12	Metallic Foil/Film	34
3.5	Parts List	10	4.5	Electronic Component Materials	36
3.6	Test Requirement Considerations	10	4.5.1	Embedded (Buried) Resistors	36
3.6.1	Electrical	10	4.5.2	Embedded (Buried) Capacitors	36
3.6.2	Printed Board Assembly Testability	12	4.5.3	Embedded (Buried Inductors)	36
3.6.3	Boundary Scan Testing	13	4.6	Organic Protective Coatings	36
3.6.4	Functional Test Concern for Printed Board Assemblies	14	4.6.1	Solder Mask Coatings	36
3.6.5	In-Circuit Test Concerns for Printed Board Assemblies	15	4.6.2	Conformal Coatings	37
3.6.6	Mechanical	17	4.6.3	Tarnish Protective Coatings	38
3.7	Layout Evaluation	17	4.7	Marking and Legends	38
3.7.1	Printed Board Layout Design	17			
3.7.2	Feasibility Density Evaluation	18			

4.7.1	ESD Considerations	39	6.4	Impedance Controls	58
5	MECHANICAL/PHYSICAL PROPERTIES	39	6.4.1	Microstrip	59
5.1	Fabrication Considerations	39	6.4.2	Embedded Microstrip	60
5.1.1	Bare Printed Board Fabrication	39	6.4.3	Stripline Properties	61
5.2	Product/Printed Board Configuration	39	6.4.4	Asymmetric Stripline Properties	61
5.2.1	Printed Board Type	40	6.4.5	Capacitance Considerations	62
5.2.2	Printed Board Size	40	6.4.6	Inductance Considerations	63
5.2.3	Printed Board Geometries (Size and Shape) ...	42	7	THERMAL MANAGEMENT	65
5.2.4	Bow and Twist	42	7.1	Cooling Mechanisms	65
5.2.5	Structural Strength	42	7.1.1	Conduction	65
5.2.6	Composite (Constraining-Core) Printed Boards	42	7.1.2	Radiation	65
5.2.7	Vibration Design	43	7.1.3	Convection	66
5.3	Assembly Requirements	44	7.1.4	Altitude Effects	66
5.3.1	Mechanical Hardware Attachment	44	7.2	Heat Dissipation Considerations	66
5.3.2	Part Support	44	7.2.1	Printed Board Housings	66
5.3.3	Assembly and Test	45	7.2.2	Individual Component Heat Dissipation	67
5.3.4	Tooling Rails for PC Card Form Factor Printed Boards	45	7.2.3	Thermal Management Considerations for Printed Board Housings	67
5.4	Dimensioning Systems	45	7.2.4	Assembly of Heatsinks to Printed Boards	68
5.4.1	Dimensions and Tolerances	45	7.2.5	Special Design Considerations for SMT Printed Board Heatsinks	69
5.4.2	Component and Feature Location	45	7.3	Heat Transfer Techniques	70
5.4.3	Datum Features	46	7.3.1	Coefficient of Thermal Expansion (CTE) Characteristics	70
5.5	Printed Board Thickness Tolerance	49	7.3.2	Thermal Transfer	70
5.6	Panelization	49	7.3.3	Thermal Matching	70
5.7	Palletization	49	7.3.4	Thermal Design Reliability	70
6	ELECTRICAL PROPERTIES	51	8	COMPONENT AND ASSEMBLY ISSUES	72
6.1	Electrical Considerations	51	8.1	General Placement Requirements	73
6.1.1	Electrical Performance	53	8.1.1	Automatic Assembly	73
6.1.2	Power Distribution Consideration	53	8.1.2	Component Placement	73
6.1.3	Circuit Type Considerations	53	8.1.3	Orientation	74
6.2	Conductive Material Requirements	56	8.1.4	Accessibility	75
6.3	Electrical Clearance	56	8.1.5	Design Envelope	75
6.3.1	B1-Internal Conductors	57	8.1.6	Component Body Centering	75
6.3.2	B2-External Conductors, Uncoated, Sea Level to 3050 m [10,007 feet]	57	8.1.7	Flush Mounting Over Conductive Areas	75
6.3.3	B3-External Conductors, Uncoated, Over 3050 m [10,007 feet]	57	8.1.8	Clearances	76
6.3.4	B4-External Conductors, with Permanent Conformal Coating (Any Elevation)	58	8.1.9	Physical Support	76
6.3.5	A5-External Conductors, with Conformal Coating over Assembly (Any Elevation)	58	8.1.10	Heat Dissipation	78
6.3.6	A6-External Component Lead/Termination, Uncoated, Sea Level to 3050 m [10,007 feet]	58	8.1.11	Stress Relief	78
6.3.7	A7-External Component Lead/Termination, with Conformal Coating (Any Elevation)	58	8.2	General Attachment Requirements	79
			8.2.1	Through-Hole	79
			8.2.2	Surface Mounting	80
			8.2.3	Mixed Assemblies	80
			8.2.4	Soldering Considerations	80
			8.2.5	Connectors and Interconnects	81

8.2.6	Fastening Hardware	83	10	GENERAL CIRCUIT FEATURE REQUIREMENTS	102
8.2.7	Stiffeners	83	10.1	Conductor Characteristics	102
8.2.8	Lands for Flattened Round Leads	84	10.1.1	Conductor Width and Thickness	102
8.2.9	Solder Terminals	84	10.1.2	Electrical Clearance	105
8.2.10	Eyelets	86	10.1.3	Conductor Routing	105
8.2.11	Special Wiring	86	10.1.4	Conductor Spacing	105
8.2.12	Heat Shrinkable Devices	87	10.1.5	Plating Thieves	105
8.2.13	Bus Bar	87	10.2	Land Characteristics	106
8.2.14	Flexible Cable	87	10.2.1	Manufacturing Allowances	106
8.3	Through-Hole Requirements	87	10.2.2	Lands for Surface Mounting	106
8.3.1	Leads Mounted in Through-Holes	87	10.2.3	Test Points	106
8.4	Standard Surface Mount Requirements	91	10.2.4	Orientation Symbols	106
8.4.1	Surface-Mounted Leaded Components	91	10.3	Large Conductive Areas	106
8.4.2	Flat-Pack Components	92	11	DOCUMENTATION	106
8.4.3	Ribbon Lead Termination	92	11.1	Special Tooling	108
8.4.4	Round Lead Termination	92	11.2	Layout	108
8.4.5	Component Lead Sockets	92	11.2.1	Viewing	108
8.5	Fine Pitch SMT (Peripherals)	93	11.2.2	Accuracy and Scale	108
8.6	Bare Die	93	11.2.3	Legend Notes	108
8.6.1	Wire Bond	93	11.2.4	Automated-Layout Techniques	108
8.6.2	Flip Chip	93	11.3	Deviation Requirements	108
8.6.3	Chip Scale	93	11.4	Phototool Considerations	109
8.7	Tape Automated Bonding	93	11.4.1	Artwork Master Files	109
8.8	Grid Array SMT	93	11.4.2	Film Base Material	109
8.9	No-Lead Devices	94	11.4.3	Solder Mask Coating Phototools	109
8.9.1	Small Outline and Quad Flat No Lead with Pullback Leads (PQFN, PSON)	94	12	QUALITY ASSURANCE	109
8.10	Compliant Pin Design Guidelines	95	12.1	Conformance Test Coupons	109
9	HOLES/INTERCONNECTIONS	95	12.2	Material Quality Assurance	110
9.1	General Requirements for Lands with Holes ..	95	12.2.1	Laminates	110
9.1.1	Land Requirements	95	12.2.2	Compliant Pin	110
9.1.2	Annular Ring Requirements	96	12.3	Conformance Evaluations	110
9.1.3	Thermal Relief in Conductor Planes	97	12.3.1	Coupon Quantity and Location	110
9.1.4	Lands for Flattened Round Leads	97	12.3.2	Coupon Identification	114
9.2	Holes	98	12.3.3	General Coupon Requirements	114
9.2.1	Unsupported Holes	98	12.4	Individual Coupon Design	114
9.2.2	Plated Holes	98	12.4.1	Plated Hole Evaluation (Thermal Stress, Rework Simulation, Registration) Coupons ..	114
9.2.3	Location	100	12.4.2	Moisture and Insulation Resistance Coupons	115
9.2.4	Hole Pattern Variation	100	12.4.3	Hole Solderability Coupons	115
9.2.5	Location Tolerances	100	12.4.4	Surface Mount Solderability Coupons	115
9.2.6	Quantity	101	12.4.5	Interconnect Resistance and Continuity Coupons	115
9.2.7	Spacing of Adjacent Holes	101	12.4.6	Solder Mask Adhesion Coupons	115
9.2.8	Aspect Ratio	101	12.4.7	Surface Insulation Resistance Coupons	115
9.3	Via Protection	101			
9.3.1	Via Protection Requirements	101			
9.3.2	Via Fill	101			

12.4.8 Peel Strength and Plating Adhesion Coupons 116

12.4.9 Controlled Impedance Coupons 116

12.4.10 Optional Legacy Registration Coupons 116

12.4.11 Legacy N Coupon (Peel Strength, Surface Mount Bond Strength - Optional for SMT) .. 116

12.4.12 Coupon X (Bending Flexibility and Endurance, Flexible Printed Board) 116

12.4.13 Process Control Test Coupon 116

APPENDIX A 117

APPENDIX B 142

APPENDIX C 162

Figures

Figure 1-1 Microvia Definition 2

Figure 3-1 Package Size and I/O Count 9

Figure 3-2 Test Land Free Area for Parts and Other Intrusions 16

Figure 3-3 Test Land Free Area for Tall Parts 16

Figure 3-4 Probing Test Lands 16

Figure 3-5 Example of Usable Area Calculation, mm [in] (Usable area determination includes clearance allowance for edge printed board connector area, printed board guides, and printed board extractor.) 18

Figure 3-6 Printed Board Density Evaluation 20

Figure 4-1 HASL Surface Topology Comparison 34

Figure 5-1 Example of Printed Board Size Standardization, mm [in] 41

Figure 5-2 Typical Asymmetrical Constraining-Core Configuration 43

Figure 5-3A Multilayer Metal Core Printed Board with Two Symmetrical Copper-Invar-Copper Constraining Cores (when the Copper-Invar-Copper planes are connected to the plated-through hole, use the minimum relief per Figure 9-4) 43

Figure 5-3B Symmetrical Constraining Core Printed Board with a Copper-Invar-Copper Center Core 43

Figure 5-4 Advantages of Positional Tolerance Over Bilateral Tolerance, mm [in] 46

Figure 5-5 Datum Reference Frame 47

Figure 5-6 Example of Location of a Pattern of Pads, mm [in] 48

Figure 5-7 Example of a Pattern of Tooling/Mounting Holes, mm [in] 48

Figure 5-8 Example of Location of a Conductor Pattern Using Fiducials, mm [in] 49

Figure 5-9 Example of Printed Board Profile Location and Tolerance, mm [in] 50

Figure 5-10 Example of a Printed Board Drawing Utilizing Geometric Dimensioning and Tolerancing, mm [in] 50

Figure 5-11 Fiducial Clearance Requirements 51

Figure 5-12 Printed Board Panelization/Palletization, mm 51

Figure 5-13 Example of Connector Key Slot Location and Tolerance, mm [in] 52

Figure 6-1 Voltage/Ground Distribution Concepts 54

Figure 6-2 Single Reference Edge Routing 55

Figure 6-3 Circuit Distribution 55

Figure 6-4 Transmission Line Printed Board Construction 59

Figure 6-5 Capacitance vs. Conductor Width and Dielectric Thickness for Microstrip Lines, mm [in] 63

Figure 6-6 Capacitance vs. Conductor Width and Spacing for Striplines, mm [in] 64

Figure 6-7 Single Conductor Crossover 64

Figure 7-1 Component Clearance Requirements for Automatic Component Insertion 68

Figure 7-2 Relative Coefficient of Thermal Expansion (CTE) Comparison 71

Figure 8-1 Component Orientation for Boundaries and/or Wave Solder Applications 75

Figure 8-2 Component Body Centering 75

Figure 8-3 Axial-Leaded Component Mounted Over Conductors 76

Figure 8-4 Unpopulated Board Clearance 76

Figure 8-5 Lamp-Mounted Axial-Leaded Component ... 76

Figure 8-6 Adhesive-Bonded Axial-Leaded Component 76

Figure 8-7 Example of Filletting Compared to Bonding .. 77

Figure 8-8 Mounting with Feet or Standoffs 77

Figure 8-9 Heat Dissipation Examples 78

Figure 8-10 Lead Bends 79

Figure 8-11 Typical Lead Configurations 79

Figure 8-12 Typical Keying Arrangement 82

Figure 8-13 Printed Board Edge Tolerancing 82

Figure 8-14 Lead-In Chamfer Configuration 83

Figure 8-15 Two-Part Connector 83

Figure 8-16 Edge-Board Adapter Connector 83

Figure 8-17 Round or Flattened (Coined) Lead Joint Description 85

Figure 8-18 Standoff Terminal Mounting, mm [in] 85

Figure 8-19 Dual Hole Configuration for Interfacial and Interlayer Terminal Mountings 86

Figure 8-20 Partially Clinched Through-Hole Leads 88

Figure 8-21 Dual In-Line Package (DIP) Lead Bends 88

Figure 8-22 Solder in the Lead Bend Radius 88

Figure 8-23 Two-Lead Radial-Leaded Components 89

Figure 8-24 Radial Two-Lead Component Mounting, mm [in] 89

Figure 8-25 Meniscus Clearance, mm [in] 89

Figure 8-26 "TO" Can Radial-Leaded Component, mm [in] 89

Figure 8-27	Perpendicular Part Mounting, mm [in]	90	Figure A.5-1	E Coupon Layout, mm [in]	126
Figure 8-28	Flat-Packs and Quad Flat-Packs	90	Figure A.5-2	E Coupon	127
Figure 8-29	Examples of Configuration of Ribbon Leads for Through-Hole Mounted Flat-Packs	90	Figure A.6-1	S Coupon Layout, mm [in]	128
Figure 8-30	Metal Power Packages with Compliant Leads	90	Figure A.6-2	S Coupon Example Layers	129
Figure 8-31	Metal Power Package with Resilient Spacers	90	Figure A.7-1	W Coupon Layout, mm [in]	130
Figure 8-32	Metal Power Package with Noncompliant Leads	90	Figure A.7-2	W Coupon Layout	131
Figure 8-33	Examples of Flat-Pack Surface Mounting	91	Figure A.8-1	D Coupon Layout with A and B Features, mm [in]	132
Figure 8-34	Round or Coined Lead	92	Figure A.8-2	D Coupon Example Layers with A and B Features	133
Figure 8-35	Configuration of Ribbon Leads for Planar Mounted Flat-Packs	92	Figure A.8-3	D Coupon Layout with Non-through Via B Features, mm [in]	133
Figure 8-36	Heel Mounting Requirements	92	Figure A.9-1	G Coupon Layout, mm [in]	135
Figure 8-37	TSSOP Package Construction	93	Figure A.9-2	G Coupon Example Layers	136
Figure 8-38	SQFP Package Construction	93	Figure A.10-1	H Coupon Layout, mm [in]	137
Figure 8-39	Examples of Ball Grid Array (BGA) Package Construction	94	Figure A.10-2	H Coupon Example Layers	138
Figure 8-40	Ceramic Column Grid Array (CGA) Package Construction	94	Figure A.11-1	P Coupon Layout, mm [in]	139
Figure 8-41	Land Grid Array (LGA) Package Construction	94	Figure A.11-2	P Coupon Example Layers	139
Figure 8-42	Quad Flat No-Lead (QFN) Construction	95	Figure A.12-1	Z Coupon Layout (Microstrip and edge-coupled microstrip), mm [in]	140
Figure 8-43	Small Outline No-lead (SON) Construction	95	Figure A.12-2	Z Coupon Example Layers	141
Figure 8-44	Pullback Quad Flat No Lead (PQFN) Construction	95	Figure A.12-3	Z Coupon Layout (Microstrip and edge-coupled microstrip using alternative test points), mm [in]	141
Figure 9-1	Examples of Modified Land Shapes	96	Figure B.2-1	Test Coupons A and B, mm [in]	143
Figure 9-2	External Annular Ring	97	Figure B.2-2	Test Coupons A and B (Conductor Detail), mm [in]	144
Figure 9-3	Internal Annular Ring	97	Figure B.2-3	Test Coupon A/B, mm [in]	145
Figure 9-4	Typical Thermal Relief in Planes	97	Figure B.2-4	Test Coupon A/B (Conductor Detail), mm [in]	146
Figure 10-1	Etched Conductor Characteristics	104	Figure B.3-1	Coupon E, mm	147
Figure 10-2	Example of Conductor Beef-Up or Neck-Down	105	Figure B.3-2	“Y” Pattern for Chip Component Cleanliness Test Pattern	147
Figure 10-3	Conductor Optimization Between Lands	105	Figure B.4-1	Test Coupon S, mm [in]	148
Figure 11-1	Flow Chart of Printed Board Design/Fabrication Sequence	107	Figure B.5-1	Test Coupon M, Surface Mounting Solderability Testing, mm [in]	149
Figure 11-2	Multilayer Printed Board Viewing	108	Figure B.6-1	Test Coupon D, mm [in]	150
Figure 11-3	Gang Solder Mask Window	109	Figure B.6-2	10 Layer Example	151
Figure 11-4	Pocket Solder Mask Window	109	Figure B.6-3	Example of a 10 Layer Coupon D, Modified to Include Blind and Buried Vias	152
Figure 12-1	Panel Utilization among IPC-2221B Conformance Coupon Designs	112	Figure B.6-4	Test Coupon D for Process Control of 4 Layer Printed Boards	153
Figure 12-2	Panel Utilization among Legacy Conformance Coupon Designs	113	Figure B.7-1	Test Coupon G, Solder Resist Adhesive, mm [in]	153
Figure 12-3	Example Stack-up for a Ten Layer Printed Board	113	Figure B.8-1	Optional Coupon H, mm [in]	154
Figure 12-4	Systematic Path for Implementation of Statistical Process Control (SPC)	116	Figure B.8-2	Comb Pattern Examples	155
Figure A.2-1	AB/R Coupon Layout, mm [in]	119	Figure B.9-1	Coupon C, External Layers Only, mm [in]	155
Figure A.2-2	AB/R Coupon Example Layers	120	Figure B.10-1	Test Coupon F, mm [in]	157
Figure A.3-1	A/R Coupon Layout, mm [in]	122	Figure B.10-2	Test Coupon R, mm [in]	158
Figure A.3-2	A/R Coupon Example Layers	123	Figure B.10-3	Worst-Case Hole/Land Relationship	158
Figure A.4-1	B/R Coupon Layout, mm [in]	125	Figure B.11-1	Test Coupon N, Surface Mounting Bond Strength and Peel Strength, mm [in]	159

Figure B.12-1	Test Coupon X, mm [in]	161
Figure B.12-2	Bending Test	161

Tables

Table 3-1	PCB Design/Performance Tradeoff Checklist	6	Table 5-3	Typical Assembly Equipment Limits	45
Table 3-2	Component Grid Areas	19	Table 6-1	Electrical Conductor Spacing	57
Table 4-1	Typical Properties of Common Dielectric Materials	23	Table 6-2	Typical Relative Bulk Dielectric Constant of Printed Board Material	60
Table 4-2	Final Finish and Coating Requirements	26	Table 6-3	Example Plane Sequences for a Six Layer Printed Board	62
Table 4-3	Surface and Hole Copper Plating Minimum Requirements for Buried Vias >2 Layers, Through-Holes, and Blind Vias	27	Table 7-1	Effects of Material Type on Construction	65
Table 4-4	Surface and Hole Copper Plating Minimum Requirements for Microvias (Blind and Buried)	27	Table 7-2	Emissivity Ratings for Certain Materials	66
Table 4-5	Surface and Hole Copper Plating Minimum Requirements for Buried Via Cores (2 Layers)	27	Table 7-3	Printed Board Heatsink Assembly Preferences	69
Table 4-6	Surface Finishes	28	Table 7-4	Comparative Reliability Matrix Component Lead/Termination Attachment	70
Table 4-7	Gold Plating Uses	29	Table 9-1	Minimum Standard Fabrication Allowance for Interconnection Lands	96
Table 4-8	ENIG Surface Finish Advantages and Disadvantages	30	Table 9-2	Annular Rings (Minimum)	97
Table 4-9	ENIG/EG Surface Finish Advantages and Limitations	30	Table 9-3	Minimum Drilled Hole Size for Buried Vias	99
Table 4-10	ENEPIG Surface Finish Advantages and Disadvantages	31	Table 9-4	Minimum Drilled Hole Size for Blind Vias	99
Table 4-11	Immersion Silver Surface Finish Advantages and Disadvantages	31	Table 9-5	Minimum Hole Location Tolerance, dtp	101
Table 4-12	Immersion Tin Surface Finish Advantages and Disadvantages	32	Table 9-6	Through-Hole Diameters Minimum and Maximum and Aspect Ratio, mm [in]	102
Table 4-13	OSP Surface Finish Advantages and Limitations	33	Table 10-1	Internal Layer Foil Thickness After Processing	103
Table 4-14	Copper Foil/Film Requirements	35	Table 10-2	External Conductor Thickness After Plating	103
Table 4-15	Metal Core Substrates	36	Table 12-1	Appendix A Coupon Requirements	111
Table 4-16	Typical Minimum Solder Mask Clearances and Dams	37	Table 12-2	Appendix B (Legacy) Coupon Requirements	111
Table 4-17	Conformal Coating Types and Thickness Range	38	Table A.1-1	IPC Coupons	117
Table 4-18	Conformal Coating Functionality	38	Table A.2-1	AB/R Coupon Parameters, mm [in]	118
Table 5-1	Fabrication Assumptions and Considerations	40	Table A.3-1	A/R Coupon Parameters, mm [in]	121
Table 5-2	PC Card Form Factor Substrate Dimensions	40	Table A.4-1	B/R Coupon Parameters, mm [in]	124
			Table A.5-1	E Coupon Parameters, mm [in]	126
			Table A.6-1	S Coupon Parameters, mm [in]	128
			Table A.7-1	W Coupon Parameters, mm [in]	130
			Table A.8-1	D Coupon Parameters, mm [in]	132
			Table A.9-1	G Coupon Parameters, mm [in]	134
			Table A.10-1	H Coupon Parameters, mm [in]	137
			Table A.11-1	P Coupon Parameters, mm [in]	139
			Table A.12-1	Z Coupon Parameters, mm [in]	140
			Table B.1-1	IPC-2221 Legacy Coupons	142

Generic Standard on Printed Board Design

1 SCOPE

This standard establishes the generic requirements for the design of organic printed boards and other forms of component mounting or interconnecting structures, including PC card form factors. The organic materials may be homogeneous, reinforced, or used in combination with inorganic materials; the interconnections may be single, double, or multilayered.

1.1 Purpose The requirements contained herein are intended to establish design principles and recommendations that **shall** be used in conjunction with the detailed requirements of a specific interconnecting structure sectional standard (see 1.2) to produce detailed designs intended to mount and connect components. This standard is not intended for use as a performance specification for finished printed boards nor as an acceptance document for electronic assemblies.

1.2 Documentation Hierarchy This standard identifies generic physical design principles, and is supplemented by various sectional standards that provide sharper focus on specific aspects of printed board technology. These include:

IPC-2222 Rigid organic printed board design
IPC-2223 Flexible printed board design
IPC-2225 Organic, MCM-L, printed board design
IPC-2226 High Density Interconnect (HDI) printed board design

The documents are a part of the Family of Design Documents which is identified as IPC-2220. The number IPC-2220 is for ordering purposes only and includes this standard and the four listed above.

Note: IPC-2224, a sectional design standard for PC card form factors, was cancelled by the IPC. Relevant PC form factor design information has been transferred to this revision of IPC-2221 and to IPC-2222.

1.3 Presentation All dimensions and tolerances in this standard are expressed in hard SI (metric) units and parenthetical soft imperial (inch) units. Users of this standard are expected to use metric dimensions. All dimensions greater than or equal to 0.1 mm [0.0039 in] will be expressed in millimeters and inches. All dimensions less than 0.1 mm [0.0039 in] will be expressed in micrometers and microinches.

1.3.1 Dimensional Units The following is taken from National Institute of Standards and Technology - Metric Information and Conversions: "Beginning January 1, 2010, the European Union Council Directive 80/181/EEC (Metric Directive) allowed the use of only metric units, and prohibited the use of any other measurements for most products sold in the European Union (EU). The Metric Directive made the sole use of metric units obligatory in all aspects of life in the European Union, extending to areas such as product literature and advertising."

Most component datasheets are provided in metric units. Many printed board designers spend a lot of time converting between imperial (inch) and SI (metric). Round-off errors, when converting units, can result in inaccuracies that result in marginal or failed designs. However, the printed board fabrication vendors often default to imperial units. Electronic Computer Aided Design (ECAD) tools accommodate both metric and imperial library components being placed on the same printed board because dimensional precision is large enough to describe most standard components accurately.

Problems arise when importing information from third party software or trying to mix units during printed board layout. For example, if a portion of the printed board design is an imported Drawing Exchange Format (.DXF) file with metric units that needs to interface with a digital portion done in imperial units, a problem can occur where the data from the two grids are mixed. Unlike importing from libraries, a conversion to printed board units is not always done when importing DXF.

While a user can convert printed board units from metric to imperial in modern day tools without problems, this should not be done too often during the design phase as repeated conversions can introduce unexpected errors. A single set of units should be used in the layout of the printed board. If imported data is in metric units, the layout portion of the process should use metric units. Once the layout is complete and verified, the designer can convert the printed board to imperial units for documentation, if necessary.

1.4 Interpretation "Shall," the imperative form of the verb, is used throughout this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a "shall" requirement may be considered if sufficient data is supplied to justify the exception.