

IEEE Standard for Adoption of MIPI Alliance Specification for A-PHY Interface (A-PHY) Version 1.0

Developed by the
IEEE Board of Governors Corporate Advisory Group (CAG)

IEEE SA Industry Affiliate Network (IAN)
base specification contributed by MIPI Alliance



IEEE Standard for Adoption of MIPI Alliance Specification for A-PHY Interface (A-PHY) Version 1.0

Developed by the

Corporate Advisory Group (BOG/CAG)
of the
IEEE SA Board of Governors

Approved 16 June 2021

IEEE SA Standards Board

Abstract: This standard adopts MIPI Alliance—MIPI A-PHY Specification Version 1.0 as an IEEE Standard. The adopted standard provides an asymmetric data link in a point-to-point or daisy-chain topology, with high-speed unidirectional data, embedded bidirectional control data and optional power delivery over a single cable. In this way, it reduces wiring, cost and weight, as high-speed data, control data and optional power share the same physical wiring. For integration with existing network backbones, it complements Ethernet, Controller Area Network (CAN), FlexRay, and other interfaces.

Keywords: 8B/10B PCS, ACMD, ACMP, adoption, advanced driver assistance systems, A-Header, A-Packet, A-Payload, APDLL, A-PHY, APPI, asymmetric, automotive, autonomous driving systems, camera, car noise, Clock Forwarding Service, coaxial cable, Control and Management System Architecture, CSE, CSI, CSI-2, descrambler, Display, DSE, DSI, DSI-2, Duplication Table, Eye Diagram, functional safety, gear, high-speed uni-directional data stream, I2C, I3C, infotainment, inline connectors, IEEE 2977, ISO 26262, jitter, Lidar, Local Functions, long reach, low-speed bi-directional command and control data, MIPI Alliance, Multi-Port, N-Z, optimal wiring cost and weight, Packet Duplication, Packet Forwarding, PAL/CSI-2, PAL/DSI-2, PAL/eDP-DP, PAL/GPIO, PAL/I2C, PAM, PAM16, PAM-X PCS, Phy, Physical layer, PML, power distribution, power over coax, Power over Differential Line, Profile, protocol adaptation layer, Radar, Routing Table, scrambler, sensor, SerDes, Serial interface, serialize, deserializer, Shielded Differential Pair (SDP), Shielded Parallel Pair (SPP), Shielded Twisted Pair (STP), test modes

The Institute of Electrical and Electronics Engineers, Inc.
3 Park Avenue, New York, NY 10016-5997, USA

Copyright © 2021 by The Institute of Electrical and Electronics Engineers, Inc.
All rights reserved. Published 25 June 2021. Printed in the United States of America.

The MIPI A-PHY specification, copyright © 2020 MIPI Alliance, Inc. and the material in Annex B excerpted from the MIPI M-PHY specification, copyright © 2017 MIPI Alliance, Inc. are reprinted with permission from MIPI Alliance, Inc.

IEEE is a registered trademark in the U.S. Patent & Trademark Office, owned by The Institute of Electrical and Electronics Engineers, Incorporated.

PDF: ISBN 978-1-5044-7698-0 STD24794
Print: ISBN 978-1-5044-7699-7 STDPD24794

IEEE prohibits discrimination, harassment, and bullying.

For more information, visit <https://www.ieee.org/about/corporate/governance/p9-26.html>.

No part of this publication may be reproduced in any form, in an electronic retrieval system or otherwise, without the prior written permission of the publisher.

Important Notices and Disclaimers Concerning IEEE Standards Documents

IEEE Standards documents are made available for use subject to important notices and legal disclaimers. These notices and disclaimers, or a reference to this page (<https://standards.ieee.org/ipr/disclaimers.html>), appear in all standards and may be found under the heading “Important Notices and Disclaimers Concerning IEEE Standards Documents.”

Notice and Disclaimer of Liability Concerning the Use of IEEE Standards Documents

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE SA) Standards Board. IEEE develops its standards through an accredited consensus development process, which brings together volunteers representing varied viewpoints and interests to achieve the final product. IEEE Standards are documents developed by volunteers with scientific, academic, and industry-based expertise in technical working groups. Volunteers are not necessarily members of IEEE or IEEE SA, and participate without compensation from IEEE. While IEEE administers the process and establishes rules to promote fairness in the consensus development process, IEEE does not independently evaluate, test, or verify the accuracy of any of the information or the soundness of any judgments contained in its standards.

IEEE does not warrant or represent the accuracy or completeness of the material contained in its standards, and expressly disclaims all warranties (express, implied and statutory) not included in this or any other document relating to the standard, including, but not limited to, the warranties of: merchantability; fitness for a particular purpose; non-infringement; and quality, accuracy, correctness, currency, or completeness of material. In addition, IEEE disclaims any and all conditions relating to results and workmanlike effort. In addition, IEEE does not warrant or represent that the use of the material contained in its standards is free from patent infringement. IEEE Standards documents are supplied “AS IS” and “WITH ALL FAULTS.”

Use of an IEEE standard is wholly voluntary. The existence of an IEEE Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEEE standard. Furthermore, the view point expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

In publishing and making its standards available, IEEE is not suggesting or rendering professional or other services for, or on behalf of, any person or entity, nor is IEEE undertaking to perform any duty owed by any other person or entity to another. Any person utilizing any IEEE Standards document, should rely upon his or her own independent judgment in the exercise of reasonable care in any given circumstances or, as appropriate, seek the advice of a competent professional in determining the appropriateness of a given IEEE standard.

IN NO EVENT SHALL IEEE BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO: THE NEED TO PROCURE SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE PUBLICATION, USE OF, OR RELIANCE UPON ANY STANDARD, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE AND REGARDLESS OF WHETHER SUCH DAMAGE WAS FORESEEABLE.

Translations

The IEEE consensus development process involves the review of documents in English only. In the event that an IEEE standard is translated, only the English version published by IEEE is the approved IEEE standard.

Official statements

A statement, written or oral, that is not processed in accordance with the IEEE SA Standards Board Operations Manual shall not be considered or inferred to be the official position of IEEE or any of its committees and shall not be considered to be, nor be relied upon as, a formal position of IEEE. At lectures, symposia, seminars, or educational courses, an individual presenting information on IEEE standards shall make it clear that the presenter's views should be considered the personal views of that individual rather than the formal position of IEEE, IEEE SA, the Standards Committee, or the Working Group.

Comments on standards

Comments for revision of IEEE Standards documents are welcome from any interested party regardless of membership affiliation with IEEE or IEEE SA. However, **IEEE does not provide interpretations, consulting information, or advice pertaining to IEEE Standards documents.**

Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Since IEEE standards represent a consensus of concerned interests, it is important that any responses to comments and questions also receive the concurrence of a balance of interests. For this reason, IEEE and the members of its Societies and Standards Coordinating Committees are not able to provide an instant response to comments, or questions except in those cases where the matter has previously been addressed. For the same reason, IEEE does not respond to interpretation requests. Any person who would like to participate in evaluating comments or in revisions to an IEEE standard is welcome to join the relevant IEEE working group. You can indicate interest in a working group using the Interests tab in the Manage Profile & Interests area of the [IEEE SA myProject system](#). An IEEE Account is needed to access the application.

Comments on standards should be submitted using the [Contact Us](#) form.

Laws and regulations

Users of IEEE Standards documents should consult all applicable laws and regulations. Compliance with the provisions of any IEEE Standards document does not constitute compliance to any applicable regulatory requirements. Implementers of the standard are responsible for observing or referring to the applicable regulatory requirements. IEEE does not, by the publication of its standards, intend to urge action that is not in compliance with applicable laws, and these documents may not be construed as doing so.

Data privacy

Users of IEEE Standards documents should evaluate the standards for considerations of data privacy and data ownership in the context of assessing and using the standards in compliance with applicable laws and regulations.

Copyrights

IEEE draft and approved standards are copyrighted by IEEE under US and international copyright laws. They are made available by IEEE and are adopted for a wide variety of both public and private uses. These

include both use, by reference, in laws and regulations, and use in private self-regulation, standardization, and the promotion of engineering practices and methods. By making these documents available for use and adoption by public authorities and private users, neither IEEE nor its licensors waive any rights in copyright to the documents.

Photocopies

Subject to payment of the appropriate licensing fees, IEEE will grant users a limited, non-exclusive license to photocopy portions of any individual standard for company or organizational internal use or individual, non-commercial use only. To arrange for payment of licensing fees, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400; <https://www.copyright.com/>. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

Updating of IEEE Standards documents

Users of IEEE Standards documents should be aware that these documents may be superseded at any time by the issuance of new editions or may be amended from time to time through the issuance of amendments, corrigenda, or errata. An official IEEE document at any point in time consists of the current edition of the document together with any amendments, corrigenda, or errata then in effect.

Every IEEE standard is subjected to review at least every 10 years. When a document is more than 10 years old and has not undergone a revision process, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE standard.

In order to determine whether a given document is the current edition and whether it has been amended through the issuance of amendments, corrigenda, or errata, visit [IEEE Xplore](#) or [contact IEEE](#). For more information about the IEEE SA or IEEE's standards development process, visit the IEEE SA Website.

Errata

Errata, if any, for all IEEE standards can be accessed on the [IEEE SA Website](#). Search for standard number and year of approval to access the webpage of the published standard. Errata links are located under the Additional Resources Details section. Errata are also available in [IEEE Xplore](#). Users are encouraged to periodically check for errata.

Patents

IEEE Standards are developed in compliance with the [IEEE SA Patent Policy](#).

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken by the IEEE with respect to the existence or validity of any patent rights in connection therewith. If a patent holder or patent applicant has filed a statement of assurance via an Accepted Letter of Assurance, then the statement is listed on the IEEE SA Website at <https://standards.ieee.org/about/sasb/patcom/patents.html>. Letters of Assurance may indicate whether the Submitter is willing or unwilling to grant licenses under patent rights without compensation or under reasonable rates, with reasonable terms and conditions that are demonstrably free of any unfair discrimination to applicants desiring to obtain such licenses.

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting

Essential Patent Claims may exist for which a Letter of Assurance has not been received. The IEEE is not responsible for identifying Essential Patent Claims for which a license may be required, for conducting inquiries into the legal validity or scope of Patents Claims, or determining whether any licensing terms or conditions provided in connection with submission of a Letter of Assurance, if any, or in any licensing agreements are reasonable or non-discriminatory. Users of this standard are expressly advised that determination of the validity of any patent rights, and the risk of infringement of such rights, is entirely their own responsibility. Further information may be obtained from the IEEE Standards Association.

This IEEE standard is based on a technical specification developed by a consortium. Patent declarations may have been provided to the consortium as a membership requirement, or in compliance with the consortium's intellectual property rights (IPR) policies and procedures. Normative references in this standard may contain material subject to patent claims that are also subject to the consortium's or other organizations' IPR policies and procedures. Additional information about declarations may be available from the consortium's website:

MIPI Alliance—[http:// www.mipi.org/](http://www.mipi.org/)

IMPORTANT NOTICE

IEEE Standards do not guarantee or ensure safety, security, health, or environmental protection, or ensure against interference with or from other devices or networks. IEEE Standards development activities consider research and information presented to the standards development group in developing any safety recommendations. Other information about safety practices, changes in technology or technology implementation, or impact by peripheral systems also may be pertinent to safety considerations during implementation of the standard. Implementers and users of IEEE Standards documents are responsible for determining and complying with all appropriate safety, security, environmental, health, and interference protection practices and all applicable laws and regulations.

Participants

At the time this IEEE standard was completed, the MIPI A-PHY Adoption Working Group had the following membership:

Richard Wietfeldt, *Chair*
Zahy Madgar, *Vice Chair*
Peter Lefkin, *Secretary*

Rob Anhofer
Rich Boyer

Hezi Saar

Leonid Smolyansky
David Woolf

The following members of the individual Standards Association balloting group voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

Philip E. Beecher
Liu Fangfang
Jefferson Hall

Daozhuang Lin
Ruben E. Salazar Cardozo
Kunal Shah

Gary Stuebing
Karl Weber
Yu Y. Chen

When the IEEE SA Standards Board approved this standard on 16 June 2021, it had the following membership:

Gary Hoffman, *Chair*
Jon Walter Rosdahl, *Vice Chair*
John D. Kulick, *Past Chair*
Konstantinos Karachalios, *Secretary*

Edward A. Addy
Doug Edwards
Ramy Ahmed Fathy
J. Travis Griffith
Thomas Koshy
Joseph L. Koepfinger*
David J. Law

Howard Li
Daozhuang Lin
Kevin Lu
Daleen C. Nohla
Chunhua Niu
Dimitris P. Povelosel
A. Bette Reilly
Dorothy Stanley

Mehmet Ulema
Lei Wang
F. Keith Waters
Karl Weber
Sha Wei
Howard Wolfman
Daidi Zhong

*Member Emeritus

Introduction

This introduction is not part of IEEE Std 2977-2021, IEEE Standard for Adoption of MIPI Alliance Specification for A-PHY Interface (A-PHY) Version 1.0.

This IEEE standard is based on a technical specification developed by a consortium. Patent declarations may have been provided to the consortium as a membership requirement, or in compliance with the consortium's intellectual property rights (IPR) policies and procedures. Normative references in this standard may contain material subject to patent claims that are also subject to the consortium's or other organizations' IPR policies and procedures. Additional information about declarations may be available from the consortium's website:

MIPI Alliance—[http:// www.mipi.org/](http://www.mipi.org/)

The A-PHY v1.0 specification was developed in 2018–2020 by member companies of the MIPI Alliance and adopted by the MIPI Board of Directors in September 2020. MIPI Alliance is a collaborative global organization serving industries that develop mobile and mobile-influenced devices.

In October 2020 a memorandum of understanding between MIPI Alliance and IEEE was announced, with the purpose of facilitating a MIPI A-PHY v1.0 adoption process within IEEE. IEEE Std 2977 is intended to bring MIPI A-PHY to a broader ecosystem beyond MIPI's membership, which in turn will foster greater interoperability, choice, and economies of scale for the global automotive industry. For IEEE, the contribution of MIPI A-PHY will add a new asymmetric approach to its existing portfolio of IEEE automotive standards.

MIPI A-PHY v1.0 is a long-reach serializer-deserializer (SerDes) physical layer interface for automotive applications, including Advanced Driver-Assistance Systems (ADAS), Automated Driving Systems (ADS), and other surround-sensor applications.

Ongoing development of the A-PHY specification will remain with MIPI Alliance.

Users should note that the only normative reference listed in the Reference clause of this adoption is to Section 4.5 of M-PHY Specification [MIPI08]. The referenced section is provided in Annex B.

Trademarks and service marks in this standard identify materials provided for the convenience of users and do not constitute an endorsement by IEEE of these products. Equivalent products may be used if they can be shown to lead to the same results.

Contents

Figures	ix
Tables	xiii
Release History.....	xvii
1 Introduction	1
1.1 Scope	1
1.1.1 In Scope	1
1.1.2 Out of Scope	1
1.2 Purpose	1
2 Terminology	2
2.1 Use of Special Terms	2
2.2 Definitions	2
2.3 Abbreviations	3
2.4 Acronyms	4
3 References	6
4 Overview	8
5 Architecture	10
5.1 High Level Structure	10
5.2 Profiles	11
5.3 Gears.....	12
5.4 Safety.....	13
6 Interconnect	15
6.1 Lane Configuration.....	15
6.2 Cable Topology	15
6.3 Boundary Conditions.....	16
6.4 S-Parameter Specification	16
6.5 Characterization Conditions	16
6.6 Interconnect Specifications	17
6.6.1 Total Interconnect	18
6.6.2 Cable TLI (Transmission Line Interconnect Structure).....	18
6.6.2.1 Characteristic Impedance	18
6.6.2.2 Insertion Loss	18
6.6.2.3 Return Loss.....	19
6.6.2.4 Coupling Attenuation.....	20
6.6.2.5 Alien Cable Bundle Crosstalk	22
6.6.3 ENIS (End Node Interconnect Structure)	23
6.6.3.1 Characteristic Impedance	23
6.6.3.2 Insertion Loss	24
6.6.3.3 Return Loss.....	25
6.6.3.4 Mode Conversion	26
6.6.3.5 Receiver Alien Near End Crosstalk.....	26

6.6.4	PCB TLIS (Transmission Line Interconnect Structure) (Informative)	27
6.6.4.1	Characteristic Impedance	28
6.6.4.2	Insertion Loss	28
6.6.4.3	Return Loss	28
6.6.5	Power Distribution	28
6.6.5.1	DC Requirements	28
6.6.5.2	AC Requirements	29
6.6.5.3	Power Over Coax	30
6.6.5.4	Power Over Differential Line	30
6.6.6	Ground Voltage Offset	31
7	EMC Environmental Conditions	32
7.1	RF Ingress	32
7.2	Bulk Current Injection (BCI)	32
7.3	Fast Transient	33
7.4	Alien Cable Bundle Max PSD Level	33
7.5	Car Noise (PSD)	34
8	PHY Layer	35
8.1	Architecture	35
8.1.1	High Level Structure	35
8.1.2	Port Specification Generalization	35
8.1.3	Master/Slave Clocking Schemes	36
8.1.4	PHY Layer Implementation Guidelines	36
8.1.4.1	A-PHY P1 G1/G2 Architecture	36
8.1.4.2	A-PHY P2 G1/G2 Architecture	37
8.1.4.3	A-PHY G3–G5 Architecture	38
8.1.5	PHY-Related A-Packet Fields	40
8.2	RTS	40
8.2.1	PAM-X Payload Data Modulation Assignment by Source	45
8.2.2	Active Message Counter Window	46
8.2.3	Retransmission Request / Ack Types	46
8.2.3.1	Retransmission Request Triggering by the Receiver	47
8.2.3.2	Retransmission Request Handling at TX RTS	48
8.2.3.3	Format of Single/Gap Retransmission Request Sent Over Downlink	48
8.2.4	Time Bounded RTS	50
8.2.5	A-Packet – PHY Related Header/Tail Modifications	51
8.2.5.1	Tx Delay	51
8.2.5.2	Message Counter and Original Indication Bit	51
8.2.5.3	Header CRC (CRC-8)	51
8.2.5.4	A-Packet Tail CRC (CRC-32)	53
8.2.6	Fully Paced A-Packet Stream from TX Data Link Layer to TX RTS	54
8.2.6.1	Max Net Link Rate for 8B/10B PCS	54
8.2.6.2	Max Net Link Rate for PAM-X PCS	54
8.2.6.3	8B/10B PCS Fully Paced, A-Packets Stream from Link to TX RTS	54
8.2.6.4	PAM-X PCS Fully Paced, A-Packets Stream from Link to TX RTS	55
8.2.7	Retransmitted A-Packets Scheduling Priority at TX RTS	56
8.2.8	RTS Bypass	56

8.3	Physical Coding Sub-Layer (PCS)	58
8.3.1	PAM-X PCS	58
8.3.1.1	PAM16 Sub-Constellation Bit to Symbol mapping	59
8.3.1.2	Symbol and Token Rate/Period	61
8.3.1.3	A-Packet to Token Conversion	63
8.3.1.4	Downlink Scrambler	65
8.3.1.5	Downlink Training Mode	66
8.3.1.6	Downlink Idle Mode	69
8.3.1.7	Downlink Normal Mode	69
8.3.1.8	Downlink JITC Re-Training	71
8.3.2	8B/10B PCS	72
8.3.2.1	10b Symbols to NRZ Mapping	73
8.3.2.2	8B/10B Encoding	73
8.3.2.3	Uplink Scrambler	73
8.3.2.4	Downlink Scrambler	74
8.3.2.5	Byte Stream Controller	74
8.3.2.6	Training Mode	75
8.3.2.7	Idle Mode	76
8.3.2.8	Normal Mode	77
8.3.3	Startup Procedure	80
8.3.3.1	“Mission Mode” Startup Procedure	81
8.3.3.2	Unidirectional Startup Procedure	83
9	PMD Electrical Specification	86
9.1	TX Electrical Specification	86
9.1.1	Test Mode Pattern Generator (TMPG)	86
9.1.1.1	LFSR Usage Example	87
9.1.2	Test Modes	89
9.1.2.1	TM1: Test Mode 1: Transmit PSD	89
9.1.2.2	TM2: Test Mode 2: Droop	89
9.1.2.3	TM3: Test Mode 3: Transmit Jitter	90
9.1.2.4	TM4: Test Mode 4: Transmit Linearity	90
9.1.2.5	TM5: Test Mode 5: In Silent State	90
9.1.2.6	TM6: Test Mode 6: Unidirectional Startup	90
9.1.3	Transmitter Power Spectral Density Mask	90
9.1.3.1	Requirement	90
9.1.3.2	Processing Procedure	94
9.1.4	Transmitter Maximum Output Droop	98
9.1.4.1	Requirement	98
9.1.4.2	Processing Procedure	98
9.1.5	Transmitter Timing Jitter	98
9.1.5.1	Requirement	98
9.1.5.2	Processing Procedure	98
9.1.6	Transmitter Symbol Rate Accuracy	99
9.1.7	NRZ Downlink Transmitter Eye Opening	99
9.1.7.1	Requirement	99
9.1.7.2	Processing Procedure	99
9.1.7.3	NRZ Jitter (Informative)	100

9.1.8	PAM-X Transmitter Linearity.....	101
9.1.8.1	Requirement	101
9.1.8.2	Processing Procedure.....	101
9.2	RX Electrical Specification.....	104
9.2.1	Profile 1 Receiver Bit Error Rate.....	104
9.2.2	Profile 2 Downlink Receiver Pre-RTS Packet Error Rate	104
9.2.3	Profile 2 Uplink Receiver Bit Error Rate.....	104
9.2.4	Receiver Symbol Rate Frequency Tolerance.....	104
9.2.5	Receiver Test Modes.....	104
9.2.5.1	RTM6: Receiver Test Mode 6: Unidirectional Startup.....	104
10	Modes of Operation.....	106
10.1	Non-Active Mode.....	106
10.2	Active Mode	106
10.3	Operation Mode State Machine.....	106
10.3.1	General Operation.....	107
10.3.2	States.....	107
10.3.2.1	Power-Up State.....	108
10.3.2.2	Start-Up State	108
10.3.2.3	Normal State.....	108
10.3.2.4	Sleep State	108
10.3.3	Transitions.....	109
10.3.3.1	Power-Off Transition.....	109
10.3.3.2	Reset Transition.....	109
10.3.3.3	Ready Transition.....	109
10.3.3.4	Stop Transition.....	109
10.3.3.5	Link Establish Transition.....	110
10.3.3.6	Link Down Transition.....	110
10.3.3.7	Sleep Transition.....	110
10.3.3.8	Wakeup Transition.....	111
10.3.4	Test Mode	111
10.4	FSM Parameters	112
10.5	Wake-Up Protocol	113
10.5.1	General.....	113
10.5.1.1	System Architecture (Informative).....	113
10.5.2	Wake-Up Pattern (WUP) Signal	116
10.5.2.1	PRBS9 Pattern.....	116
10.5.2.2	WUP Amplitude	116
10.5.2.3	WUP Bit Rate.....	117
10.5.2.4	WUP Duration	117
10.5.2.5	WUP Generation.....	117
10.5.2.6	WUP Detection.....	117
10.5.3	WUP Handshake Procedure.....	117
10.5.4	WUP Parameters	118

11	Data Link Layer	119
11.1	Architecture Overview	119
11.2	A-Packet Format.....	121
11.2.1	A-Packet Header (A-Header) Fields.....	122
11.2.1.1	Adaptation Descriptor Field	123
11.2.1.2	Service Descriptor Field.....	123
11.2.1.3	Placement Descriptor Field	126
11.2.1.4	PHY2 Field.....	126
11.2.1.5	Target Address Field.....	126
11.2.1.6	PHY3 Field.....	128
11.2.1.7	Payload Length Field.....	128
11.2.1.8	PHY Header CRC Field.....	128
11.2.2	A-Packet Payload (A-Payload).....	128
11.2.3	A-Packet Tail (A-Tail) (CRC-32 Field)	128
11.3	Link Service	129
11.3.1	BIST A-Packet	129
11.3.1.1	BIST Modes.....	129
11.3.1.2	BIST Payload Patterns.....	129
11.3.1.3	BIST Rate	129
11.3.1.4	BIST Burst.....	130
11.3.2	Keep-Alive.....	130
11.3.3	Remote Sleep Command	130
11.4	Local Functions	131
11.4.1	Local Table (LOC_TBL) Recommendations (Informative)	131
11.5	Multi-Port Functions	133
11.5.1	Multi-Port Routing Function	134
11.5.1.1	Packet Duplication Stage.....	134
11.5.1.2	Packet Forwarding Stage.....	134
11.5.1.3	Routing Table (ROUT_TBL) Recommendations (Informative)	135
11.5.1.4	Duplication Table (DUP_TBL) Recommendations (Informative)	135
11.6	Network Functions	137
11.6.1	Scheduling and Priorities.....	137
11.6.2	Clock Forwarding Service	137
11.6.2.1	CFS A-Packet Format.....	137
11.7	APPI Signal Interface.....	138
11.7.1	Signals Description.....	139
11.7.1.1	APPI Signals.....	139
11.7.2	APPI Clock.....	140
11.7.3	APPI A-Packet Mapping.....	141
11.7.4	APPI Timing Diagrams.....	141

12	A-PHY Control and Management Database (ACMD) and Protocol (ACMP)..	144
12.1	Control and Management System Architecture (Informative)	145
12.2	ACMD	146
12.2.1	Register Base Address Alignment	146
12.2.2	Register Data Byte Order	146
12.2.3	Register Space	147
12.2.4	Register List	148
12.2.5	Detailed Register Description	150
12.2.5.1	ACMD Programming	150
12.2.5.2	Port Programming	154
12.3	ACMP	160
12.3.1	ACMP Message Format	161
12.3.1.1	ACMP Message Header Part	161
12.3.1.2	ACMP Message Payload Part	162
12.3.1.3	ACMP Message Mapping to I ² C	164
12.3.2	ACMP Message Receiver Rules and Responsibilities	165
12.3.2.1	ACMP Header CRC (HCRC) Errors	165
12.3.2.2	ACMP Payload CRC (PCRC) Errors	165
12.3.2.3	Message Counter (MC)	165
12.3.2.4	Keep-Alive	165
12.3.2.5	Message Format Setting	165
12.3.2.6	Virtual Base Address Maintenance	165
12.3.2.7	Accessing Register Data	165
12.3.3	ACMP Interrupts	165
12.3.3.1	ACMPI in I ² C	166
12.3.3.2	ACMPI in I3C	166
Annex A	PMD Simplified Implementation Examples (Informative).....	167
A.1	Profile 1 G1–2 Source PMD	167
A.1.1	PMD without External Diplexer (Internal Replica)	167
A.1.2	PMD With External Diplexer	167
A.2	Profile 1 G1–2 Sink PMD	168
A.3	G3–5 Source PMD	168
A.4	G3–5 Sink PMD	169
Participants	171

Figures

Figure 1 Data and Power Logical Structure	8
Figure 2 High Level Layer Structure.....	8
Figure 3 A-PHY High Level Structure	11
Figure 4 A-PHY Interconnect.....	15
Figure 5 Cable Topologies.....	16
Figure 6 Set-up for S-parameter Characterization of End Nodes and TLIS.....	17
Figure 7 Interconnect Test Points Definition.....	18
Figure 8 Coax and SDP Cable Insertion Loss Limits.....	19
Figure 9 Cable TLIS Return Loss Limits	20
Figure 10 Cable TLIS Coupling Attenuation	21
Figure 11 Cable TLIS Attenuation Limits	22
Figure 12 Alien Cable Bundle Crosstalk Limit	23
Figure 13 Single-Ended End Node Routing Example.....	24
Figure 14 End Node Insertion Loss Limit.....	25
Figure 15 End Node Return Loss Limits.....	26
Figure 16 Receiver ANEXT Limit	27
Figure 17 PCB-Based Interconnect	28
Figure 18 Power Ripple Gain Function.....	29
Figure 19 Power Over Coax (PoC) Configuration	30
Figure 20 Power Over Differential Line (PoDL) Configuration	30
Figure 21 Examples of Applicable Pulses	32
Figure 22 P2 Decaying Sawtooth Model at 40 MHz / 4 nS Tr / 150 mV to 15 mV in 150 nS.....	33
Figure 23 Alien Bundle PSD Limit Line.....	34
Figure 24 A-PHY Unified Architecture.....	35
Figure 25 A-PHY P1 G1/G2 Architecture	37
Figure 26 A-PHY P2 G1/G2 Architecture	38
Figure 27 A-PHY P2 G4/G5 Architecture	39
Figure 28 Dynamically Modulated, Time Bounded, Local Retransmission	41
Figure 29 TX RTS Over 8B/10B PCS Block Diagram	42
Figure 30 TX RTS Over PAM-X PCS Block Diagram	43
Figure 31 Single Retransmission Request Sent Over Downlink.....	50

Figure 32 Gap Retransmission Request Sent Over Downlink	50
Figure 33 Header CRC (CRC-8) Bit Level Diagram	52
Figure 34 Header CRC Bit Assignment	52
Figure 35 CRC-32 Calculation Bit Level Diagram	53
Figure 36 CRC-32 Byte Mapping	53
Figure 37 Fully Paced TX Link to TX Phy Interface	56
Figure 38 RTS Bypass	58
Figure 39 PCS Block Diagram	59
Figure 40 PAM16 Sub-Constellations	60
Figure 41 A-Packet Partitioning	63
Figure 42 Bit/Symbol/Token Conversion Per Header Sub-Constellation	64
Figure 43 Bit/Symbol/Token Conversion Per Payload Data and CRC-32 Bytes	65
Figure 44 Downlink TX Scrambler LFSR	66
Figure 45 PAM-X Transition from Training to Idle	68
Figure 46 PAM-X Transition from Idle to Normal	69
Figure 47 PCS Normal Mode Data Example	70
Figure 48 TX Re-Training Procedure State Machine	71
Figure 49 PCS Block Diagram	72
Figure 50 Uplink TX Scrambler LFSR	73
Figure 51 Training with K-Sequences Example	76
Figure 52 DHA Startup Control Sequence	76
Figure 53 In_Idle Startup Control Sequence	76
Figure 54 Interrupting Request with Data Packet Continues	77
Figure 55 In Normal Startup Control Sequence	77
Figure 56 Re-Train Request	78
Figure 57 sCMax Request	78
Figure 58 Single Retransmission Request	78
Figure 59 Retransmission Gap Request	79
Figure 60 Ack Indication	79
Figure 61 Distinct A-Packet 8B/10B Encapsulation	79
Figure 62 Back-to-Back A-Packets: 8B/10B Encapsulation	79
Figure 63 A-Packet 8B/10B Encapsulation with Request Insertion	80
Figure 64 Typical Startup Procedure	81

Figure 65 Unidirectional Startup Procedure.....	85
Figure 66 TPA Conformance Point.....	86
Figure 67 Test Mode Pattern Generator LFSR.....	86
Figure 68 Test Mode 2.....	90
Figure 69 NRZ PMD: Upper & Lower PSD Limits.....	92
Figure 70 Uplink PMD Upper & Lower PSD Limits: Gears #1–#3	93
Figure 71 PAM-X PMD Upper & Lower PSD Limits	94
Figure 72 Example Matlab Figure #1.....	97
Figure 73 Example Matlab Figure #2.....	97
Figure 74 NRZ Downlink Transmitter Eye Diagram	100
Figure 75 A-PHY Port Operation Mode State Machine.....	106
Figure 76 Sleep Sequence Example, View 1	110
Figure 77 Sleep Sequence Example, View 2.....	111
Figure 78 Optional System Architecture	114
Figure 79 WUP Directions	115
Figure 80 Wakeup_ind Configuration Signaling.....	116
Figure 81 General Waveform of Main Signals.....	116
Figure 82 WUP Handshake ACK/NACK.....	117
Figure 83 A-PHY High Level Structure	119
Figure 84 Example A-PHY High-Level Layer	120
Figure 85 A-Packet Format	121
Figure 86 Bad Packet Indication and Propagation Example	125
Figure 87 Many-to-One Target Address Assignment Example	127
Figure 88 One-to-Many Target Address Assignment Example	127
Figure 89 Local Table Example.....	131
Figure 90 Entry-Element Formats	133
Figure 91 Local Table Example.....	133
Figure 92 ROUT_TBL Example	135
Figure 93 DUP_TBL Example	136
Figure 94 CFS A-Packet Payload Format	137
Figure 95 APPI Connectivity.....	140
Figure 96 APPI A-Packet Mapping	141
Figure 97 APPI Timing.....	142

Figure 98 A-PHY Control and Data Planes	144
Figure 99 Control and Management System Architecture	145
Figure 100 ACMD Register Space	147
Figure 101 Ports and AL Instances Register Space Arrangement	148
Figure 102 ACMP Message Format	161
Figure 103 Message Mapping to I ² C	164
Figure 104 Profile 1 G1–2 Source with Internal Replica	167
Figure 105 Profile 1 G1–2 Source with External Diplexer	167
Figure 106 Profile 1 G1–2 Sink PMD	168
Figure 107 G3–5 Source PMD	168
Figure 108 G3–5 Sink PMD	169

Tables

Table 1 A-PHY Gears Per Profile.....	12
Table 2 Cable TLIS Return Loss.....	20
Table 3 Coupling Attenuation.....	21
Table 4 Screening Attenuation.....	21
Table 5 Unbalanced Attenuation.....	22
Table 6 Alien Cable Bundle Crosstalk.....	23
Table 7 End Node Insertion Loss	24
Table 8 End Node Return Loss.....	25
Table 9 Receiver ANEXT.....	27
Table 10 DC Requirements	28
Table 11 Power Ripple Gain.....	29
Table 12 Power Over Coax (PoC) Component Values.....	30
Table 13 Power Over Differential Line (PoDL) Component Values.....	31
Table 14 Alien Cable Bundle Upper PSD Limit.....	33
Table 15 Car Noise PSD Limits	34
Table 16 A-Packet Fields Modified by PHY Layer.....	40
Table 17 Sub-Constellation Assignment for Original A-Packets	45
Table 18 SCI Code Per Assigned Payload Data Sub-Constellation	45
Table 19 A-Packet Fields Modified by PHY Layer.....	49
Table 20 Downlink Per Gear Max RTS Delay & Retransmission Request Wait	50
Table 21 Nominal Per Gear RTS Delay Unit	51
Table 22 Actual Byte Period Consumption Per Gear	55
Table 23 P1 A-Packet Fields Update	57
Table 24 PAM16 Sub-Constellations.....	61
Table 25 Token Data (TD) per Sub-Constellation.....	61
Table 26 Symbol / Token Rate and Symbol / Token Period Ratios.....	62
Table 27 Header Sub-Constellation Per sCMax.....	63
Table 28 Token Data Scrambling	66
Table 29 Scrambler Output Training Bits.....	67
Table 30 PAM-X "K Sequence" Symbol Mapping vs Training Symbols	67
Table 31 Idle Bits Allocation.....	69

Table 32 PAM-X EOI Symbol Allocation	69
Table 33 TX Re-Training Procedure State Machine Sequence-Length Values	71
Table 34 NRZ Electrical Levels Mapping.....	73
Table 35 8B/10B Encoding	73
Table 36 Startup Control Nibbles	74
Table 37 Normal Control Nibbles	75
Table 38 Handshake Indications for Typical Startup (Summary).....	83
Table 39 Time Periods for Startup Procedures	83
Table 40 Timer Values for Unidirectional Startup Procedure.....	84
Table 41 PAM-X Test Mode Pattern Generator LFSR Bit Allocation for Sub-Constellation	87
Table 42 LFSR Output of First 5 Symbol Periods.....	87
Table 43 sC16 ₁₆ Coding.....	87
Table 44 sC8 ₁₆ Coding.....	88
Table 45 sC4 ₁₆ Coding.....	89
Table 46 sC2 ₁₆ Coding.....	89
Table 47 Nominal TX Amplitude Over Coax, Per Gear, Per Direction (Informative)	91
Table 48 NRZ PMD Upper PSD Limit	91
Table 49 NRZ PMD Lower PSD Limit.....	91
Table 50 Uplink PMD Upper PSD Limit	92
Table 51 NRZ PMD Lower PSD Limit.....	93
Table 52 Transmitter Timing Jitter Requirements	98
Table 53 NRZ Downlink Eye Mask Parameters	99
Table 54 Jitter Components in TM3 and TM4	101
Table 55 Selection of RTM6 Sub-Mode via Field TMDData	104
Table 56 Transition Appearance Legend	107
Table 57 FSM Configuration Parameters	112
Table 58 Link Quality Code Levels.....	113
Table 59 WUP Parameters.....	118
Table 60 A-Packet Fields and Sub-Fields Description	122
Table 61 Adaptation Type Sub-Field Values.....	123
Table 62 Prio Sub-Field Values (Scheduling-Priority Codes)	123
Table 63 Quality-of-Service Codes	124
Table 64 OB (Odd-Bytes) Sub-Field Values	126

Table 65 Order Sub-Field Values.....	126
Table 66 Target Address Field Values (Pre-Defined T-Address Values).....	127
Table 67 A-Packet Payload Length and OB Sub-Field	128
Table 68 BIST Mode Codes	129
Table 69 BIST Payload Pattern Codes	129
Table 70 BIST Rate Codes	130
Table 71 BIST Burst Codes	130
Table 72 Local Table Entry Descriptor.....	132
Table 73 Duplication Stage Actions	134
Table 74 Pre-Defined Port ID Values	134
Table 75 DUP_TBL Entry Elements	136
Table 76 APPI Signals	139
Table 77 APPI Clock Frequency Settings.....	140
Table 78 Register Base Address (BA) Alignment	146
Table 79 Register Data Byte Order.....	146
Table 80 ACMD Space Register List	148
Table 81 Port Space Register List	150
Table 82 Register ACMP_VER.....	150
Table 83 Register ACMP_ADDRESS.....	151
Table 84 Register PORT_NUM.....	151
Table 85 Register AL_NUM	151
Table 86 Register ID6_HIGH.....	151
Table 87 Register ID6_LOW.....	151
Table 88 Register MID	151
Table 89 Register PRODUCT_ID.....	152
Table 90 Register ACMP_IF	152
Table 91 Register ACMP_SECONDADDR.....	152
Table 92 Register ACMP_BRDCSTADDR	152
Table 93 Register BIST_CTRL1	153
Table 94 Register BIST_CTRL2	153
Table 95 Register BIST_CTRL3	153
Table 96 Register BIST_CTRL4	153
Table 97 Register BIST_CTRL5	154

Table 98 Register INST_DESC.....	154
Table 99 Register PORT_CAP	154
Table 100 Register PORT_CONFIG	156
Table 101 Register TEST_CONFIG.....	156
Table 102 Register FSM_CONFIG	157
Table 103 Register FSM_STATUS.....	157
Table 104 Register WUP_CTRL.....	158
Table 105 Register DIAG_CTRL.....	158
Table 106 Register DIAG_CNT1	158
Table 107 Register DIAG_CNT2	159
Table 108 Register DIAG_CNT3	159
Table 109 Register DIAG_CNT4.....	159
Table 110 Register DIAG_CNT5	159
Table 111 Register DIAG_CNT6	159
Table 112 Register DIAG_CNT7	159
Table 113 Register DIAG_CNT8	160
Table 114 Register DIAG_CNT9	160
Table 115 Register DIAG_CNT10	160
Table 116 Register DIAG_CNT11	160
Table 117 Register DIAG_CNT12	160
Table 118 ACMP Message Header Fields	161
Table 119 ACMP Message Payload Fields.....	162

Release History

Date	Version	Description
06-Aug-2020	v1.0	Initial Board adopted release.

This page intentionally left blank.

1 Introduction

1 This document specifies MIPI A-PHY, a serial interface technology with high bandwidth capabilities
2 developed particularly for long reach (e.g., automotive) applications, enabling low pin count and a high level
3 of power efficiency.

4 A-PHY is designed for a wide range of long reach applications, and specifically for automotive market, to
5 carry multiple protocols from MIPI Alliance such as CSI-2 for cameras, and DSI and DSI-2 for displays.
6 Non-MIPI protocols are also supported using a generic Data Link Layer Interface (APPI).

7 A-PHY features include:

- 8 • Long reach capability – optimized to support cables up to 15 m with up to 4 inline connectors
- 9 • Multiple speed gears ranging from 2 Gbps up to 16 Gbps
- 10 • Support for multiple cable types commonly used in automotive
- 11 • Strong noise immunity for the harsh automotive environment
- 12 • Generic Data Link Layer, supporting multiple protocols from MIPI Alliance and external entities

1.1 Scope

1.1.1 In Scope

13 This A-PHY Specification document specifies the implementation of the A-PHY, including its layering,
14 electrical characteristics, and its optional features.

1.1.2 Out of Scope

15 **Protocol Adaptation Layers (PALs)**

16 A single A-PHY can serve multiple protocols at the same time, and each protocol has its own interface to the
17 Data Link Layer, called a Protocol Adaptation Layer (PAL). PALs are not part of this document.

18 **Specific Channel Configurations**

19 Different protocols employing A-PHY technology can have different constraints, which can require the use
20 of different approaches for operation control. Therefore, while this document provides the features to enable
21 stable, optimized Link configuration, it does not mandate specific configurations for specific channels.

1.2 Purpose

22 Long reach devices, and specifically automotive devices, face increasing bandwidth demands for each of
23 their functions, as well as an increase in the number of functions integrated into the system.

24 Addressing this demand requires wide bandwidth, low pin count (serial), highly power-efficient (network)
25 interfaces with sufficient flexibility to be attractive for multiple applications, while employing just a single
26 physical layer technology.

27 A-PHY complements MIPI Alliance's existing D-PHY and C-PHY interfaces by addressing the long reach
28 automotive channel.