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IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

IEEE Computer Society

Developed by the
Test Technology Standards Committee

IEEE 1838™-2019

STANDARDS

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IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

Developed by the

Test Technology Standards Committee
of the
IEEE Computer Society

Approved 7 November 2019

IEEE SA Standards Board

Abstract: IEEE Std 1838 is a die-centric standard; it applies to a die that is intended to be part of a multi-die stack. This standard defines die-level features that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks in both pre-packaging, post-packaging, and board-level situations. The primary focus of inter-die interconnect technology addressed by this standard is through-silicon vias (TSVs); however, this does not preclude its use with other interconnect technologies such as wire-bonding.

Keywords: 3D test access, flexible parallel port, FPP, IEEE 1838, multi-tower stack, primary test access port, scan, secondary test access port, test, through-silicon via, TSV

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Introduction

This introduction is not part of IEEE Std 1838-2019, IEEE Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits.

Advancements in interconnect, assembly, and packaging technology have lead to a wide range of multi-die stack architectures. These die stacks need to be tested before they can be shipped with acceptable quality levels to customers. Consequently, three-dimensional design-for test (3D-DfT) structures that provide test access between the external stack I/Os and the various dies and inter-die interconnect are needed. Test access is needed for manufacturing phases that include both partially assembled and complete stacks. This standard addresses these issues.

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1. Overview

1.1 Scope

IEEE Std 1838™-2019 standardizes mandatory and optional on-chip hardware components for 3D test access. It is intended that in the future a standard is developed for a formal, computer-readable language in which implementation choices for the three-dimensional design-for-test (3D-DfT) hardware can be specified and described. An idea of a language/data structure has been described in [B5].[1]

The aim of IEEE Std 1838 is to define at die-level standardized and scalable 3D-DfT features based on and working with digital scan-based test access, such that when compliant dies are stacked, a stack-level 3D-DfT test access architecture emerges with a minimum functionality and many optional extensions. IEEE Std 1838 provides a modular test access architecture, in which dies and interconnect layers between adjacent stacked dies can be tested individually. The focus of the standard is testing the intra-die circuitry as well as the inter-die interconnects in pre-bond, mid-bond, and post-bond cases in pre-packaging, post-packaging, and board-level situations. The standard provides test access via a mandatory one-bit (‘serial’) input/output test port and optional multi-bit (‘parallel’) test ports.

The standard is die-centric, i.e., compliance to the standard pertains to a die (and not to a stack of dies). Standardized die-level design-for-test (DfT) features comprise a stack-level test access architecture. In this way, the standard enables interoperability between die makers and stack maker.

The standard does not address stack-level challenges and solutions. The most prominent example of this is that the standard does not address compliance of the stack to IEEE Std 1149.1™ boundary scan for board-level interconnect testing (although the standard certainly does not prohibit application thereof).[2]

IEEE Std 1838 does not mandate specific defect or fault models, specific test generation methods, nor specific die-internal 2D-DfT features. However, the standard leverages existing 2D-DfT wherever applicable and appropriate, including test access ports (such as specified in IEEE Std 1149.1), on-chip DfT such as internal scan chains and wrappers of embedded cores (such as specified in IEEE Std 1500™), and on-chip design-for-debug and embedded instruments (such described in IEEE Std 1687™).

Stacking of dies requires that the vertical interconnects [e.g., micro-bumps and through-silicon vias (TSVs)] are aligned with respect to footprint (i.e., matching *x*,*y* layout locations), mechanical properties (i.e.,

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[1] The numbers in brackets correspond to those of the bibliography in Annex B.

[2] Information on references can be found in Clause 2.