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IEEE Standard for Fault Accounting and Coverage Reporting (FACR) for Digital Modules

IEEE Computer Society

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IEEE Standard for Fault Accounting and Coverage Reporting (FACR) for Digital Modules

Sponsor

Test Technology Standards Committee
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IEEE Computer Society

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Abstract: Aspects of fault models as they are relevant to the generation of test patterns for digital circuits are formalized in this standard. Fault counting, fault classification, and fault coverage reporting across different automatic test pattern generation (ATPG) tools, for the single stuck-at fault model are included in the scope. It shall be incumbent for fault coverage to be reported in a uniform way on all ATPG tools (that comply with this standard). The generation of a uniform coverage (and, hence, a uniform test quality) metric for large chips [including systems-on-chips (SOCs)] with different cores and modules for which test patterns have been independently generated will be facilitated by this standard.

Keywords: ATPG, fault models, fault simulation, IEEE 1804™, semiconductor testing, stuck-at faults, test coverage

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Introduction

This introduction is not part of IEEE Std 1804-2017, IEEE Standard for Fault Accounting and Coverage Reporting (FACR) for Digital Modules.

Like any manufacturing process, digital circuits are susceptible to various defects. Shorted or open wire connections are common defect examples. Leakier gate to drain channel in a transistor is one example of a complex defect. Fault models are defined to abstract and represent various defect mechanisms. The fault models allow automatic test pattern generation (ATPG) during the digital circuit design phase using a process called Fault Simulation. Fault Grading is the process of gauging the effectiveness of ATPG in detecting the modeled faults. The most common and prevalent fault model is the single stuck-at fault model—primarily due to its simplicity and effectiveness in representing a large class of physical defects.

The standard formalizes aspects of fault models as they are relevant to the generation of test patterns for digital circuits. Its scope includes a) fault counting, b) fault classification, and c) fault coverage reporting across different ATPG tools for the single stuck-at fault model. With this standard, it shall be incumbent on all ATPG tools (that comply with this standard) to report fault coverage in a uniform way. This can facilitate the generation of a uniform coverage (and hence a test quality) metric for large chips with different cores and modules, for which test patterns have been independently generated.

The framework established by the standard should also allow developing fault accounting standards for other fault models in the future. This may include delay defects and reliability failures while including different ways of representing digital circuits, such as VHDL, and with different levels of abstraction.

Contents

IEEE Standard for Fault Accounting and Coverage Reporting (FACR) for Digital Modules

1. Overview

1.1 Scope

This standard formalizes aspects of the stuck-at fault model as they are relevant to the generation of test patterns for digital circuits. Its scope includes a) fault counting, b) fault classification, and c) fault coverage reporting across different automatic test pattern generation (ATPG) tools for the single stuck-at fault model. Fault grading and simulation is limited to the Verilog gate level representation of a digital circuit. With this standard, it shall be incumbent on all ATPG tools (that comply with this standard) to report fault coverage in a uniform way. This can facilitate the generation of a uniform coverage (and hence a test quality) metric for large chips with different cores and modules, for which test patterns have been independently generated using an ATPG tool, or have been supplied externally and have been simulated using an ATPG tool to ascertain the fault coverage.

1.2 Purpose

Digital circuits have various structural representations either in high-level hardware description languages (HDLs), which can then be synthesized, or in netlist forms. Commercial tools today for ATPG, using algorithmic techniques, operate on a structural netlist of the design under test (DUT). The test quality signoff process mandatorily includes a minimal coverage requirement, to be obtained using these ATPG tool generated patterns on the DUT. This motivates the need for standard processes for:

a) counting faults across different fault models

b) classifying these faults

c) reporting the coverage across different ATPG tools that are used to generate test patterns for these digital circuits

Such standard processes should enable test qualification based on ATPG tool generated patterns and based upon fault coverage metrics in a uniform way and independent of the ATPG tool used. A uniform fault coverage and pattern count based metric can now be generated for large chips with complex functionality. Such metrics are commonly used in today's system-on-chips (SOCs) with a heterogeneous mix of modules therein, often consisting of intellectual property (IP) cores (which are often sourced from design teams different from those designing the chips themselves), and test patterns which are generated using different ATPG tools. This points to the need for such a standard.