IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language

IEEE Computer Society

Sponsored by the
Design Automation Standards Committee

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IEEE Std 1800™-2009
(Revision of
IEEE Std 1800-2005)

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Approved 11 November 2009
IEEE-SA Standards Board

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Abstract: This standard represents a merger of two previous standards: IEEE Std 1364™-2005 Verilog hardware description language (HDL) and IEEE Std 1800-2005 SystemVerilog unified hardware design, specification, and verification language. The 2005 SystemVerilog standard defines extensions to the 2005 Verilog standard. These two standards were designed to be used as one language. Merging the base Verilog language and the SystemVerilog extensions into a single standard provides users with all information regarding syntax and semantics in a single document.

Keywords: assertions, design automation, design verification, hardware description language, HDL, HDVL, PLI, programming language interface, SystemVerilog, Verilog, VPI

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Introduction

This introduction is not a part of IEEE Std 1800-2009, IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language.

The purpose of this standard is to provide the electronic design automation (EDA), semiconductor, and system design communities with a well-defined and official IEEE unified hardware design, specification, and verification standard language. The language is designed to coexist and enhance the hardware description and verification languages (HDVLs) presently used by designers while providing the capabilities lacking in those languages.

SystemVerilog is a unified hardware design, specification, and verification language based on the Accellera SystemVerilog 3.1a extensions to the Verilog HDL [B3][a], published in 2004. Accellera is a consortium of EDA, semiconductor, and system companies. IEEE Std 1800 enables a productivity boost in design and validation and covers design, simulation, validation, and formal assertion-based verification flows.

SystemVerilog enables the use of a unified language for abstract and detailed specification of the design, specification of assertions, coverage, and testbench verification based on manual or automatic methodologies. SystemVerilog offers application programming interfaces (APIs) for coverage and assertions, a vendor-independent API to access proprietary waveform file formats, and a direct programming interface (DPI) to access proprietary functionality. SystemVerilog offers methods that allow designers to continue to use present design languages when necessary to leverage existing designs and intellectual property. This standardization project will provide the VLSI design engineers with a well-defined IEEE standard, which meets their requirements in design and validation, and which enables a step function increase in their productivity. This standardization project will also provide the EDA industry with a standard to which they can adhere and which they can support in order to deliver their solutions in this area.

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[a]The numbers in brackets correspond to the numbers in the bibliography in Annex R.

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Participants

The **SystemVerilog Language Working Group** is entity based. At the time this standard was completed, the SystemVerilog Working Group had the following membership:

Karen Pieper, Accellera Representative, Tabula, Inc., *Chair*
Neil Korpusik, Sun Microsystems, Inc., *Vice Chair*
Johny Srouji, Apple Computer, Inc., *Chair emeritus*
Dennis Brophy, Mentor Graphics Corporation, *Secretary*
Neil Korpusik, Sun Microsystems, Inc., *Technical Chair*
Stuart Sutherland, Sutherland HDL, Inc., *Technical Editor*

Charles Dawson, Cadence Design Systems, Inc.
Yossi Levi, Intel Corporation
Mehdi Mohtashemi, Synopsys, Inc.

Work on this standard was divided among primary committees.

The **Champions Committee** was responsible for ensuring consistency in the work done by each committee.

Neil Korpusik, Sun Microsystems, Inc., *Chair*
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The **Basic/Design Committee (SV-BC)** was responsible for the specification of the design features of SystemVerilog.

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The **C API Committee (SV-CC)** was responsible for on the specification of the DPI, the SystemVerilog Verification Procedural Interace (VPI), and the additional coverage API.

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The **Special Committee (SV-SC)** was responsible for defining the new checker constructs, while also maintaining consistency among checkers, assertions, and other aspects of SystemVerilog.

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The following members of the entity balloting committee voted on this standard. Balloters may have voted for approval, disapproval, or abstention.

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1. Overview

1.1 Scope

This SystemVerilog standard (IEEE Std 1800) is a Unified Hardware Design, Specification, and Verification language. IEEE Std 1364™-2005 Verilog is a design language. Both standards were approved by the IEEE-SASB in November 2005. This standard creates new revisions of the IEEE 1364 Verilog and IEEE 1800 SystemVerilog standards, which include errata fixes and resolutions, enhancements, enhanced assertion language, merger of Verilog Language Reference Manual (LRM) and SystemVerilog 1800 LRM into a single LRM, integration with Verilog-AMS, and ensures interoperability with other languages such as SystemC and VHDL.

1.2 Purpose

The purpose of this project is to provide the EDA, Semiconductor, and System Design communities with a solid and well-defined IEEE Unified Hardware Design, Specification and Verification standard language, while resolving errata and developing enhancements to the current IEEE 1800 SystemVerilog standard. The language is designed to co-exist, be interoperable, possibly merge, and enhance those hardware description languages presently used by designers.

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