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# IEEE Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP)

IEEE Computer Society

Sponsored by the
Design Automation Standards Committee

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3 Park Avenue
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USA

**IEEE Std 1735™-2014**
(Incorporates
IEEE Std 1735-2014/Cor 1-2015)

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**Abstract:** Guidance on technical protection measures to those who produce, use, process, or standardize the specifications of electronic design intellectual property (IP) are provided in this recommended practice. Distribution of IP creates a risk of unsanctioned use and dilution of the investment in its creation. The measures presented here include protection through encryption, specification, and management of use rights that have been granted by the producers of electronic designs, and methods for integrating license verification for granted rights.

**Keywords:** digital envelope, encrypted IP, IEEE 1735™, keys, rights management, trust model

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# Introduction

This introduction is not part of IEEE Std 1735™-2014, IEEE Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP).

The purpose of this recommended practice is to provide guidance on protection of *electronic design intellectual property* (IP). The audience for this standard includes IP producers, IP consumers, vendors of tools that process protected IP, and standards development groups for IP specification formats.

When the electronic design automation (EDA) industry began creating standards for use in specifying, simulating, and implementing electronic circuits, there was no active market for the exchange of electronic designs. As interest in software reuse developed, the EDA industry began to share design collateral as a means of controlling the cost of development and managing the timeline for completing their design projects. Because that shared IP had a measurable development cost, business leaders began to insist on recovering those costs through licensing to other potential uses. Technical measures for IP protection were developed to augment the legal contracts that governed such shared use.

As the means for technical protection of IP proliferated, there was increased pressure to incorporate that technology in the existing standards for representation of IP. Expertise in protection technologies (such as encryption) was scarce in those standards development organizations (SDOs), which resulted in a slow pace of development within a given standard and technical divergence as independent organizations attempted to solve similar problems. As the marketplace for IP exchange continued to mature, concerns about technical protection of IP extended to include an interest in defining and managing the scope of use for protected IP.

This standard has been created to consolidate EDA industry efforts to unify the technical protections for IP and to guide SDOs in aligning their work for interoperability and compatibility. It is also intended to share best practices in IP protection for those who use standards that incorporate such technology, such as VHDL (IEC 61691-1-1, IEEE Std 1076™) and SystemVerilog (IEEE Std 1800™).[a]

Corrections were made to 7.4.3 as required by IEEE Std 1735-2014/Cor 1-2015.

[a]Information on references can be found in Clause 2.

# Contents

# IEEE Recommended Practice for Encryption and Management of Electronic Design Intellectual Property (IP)



## 1. Overview

### 1.1 Scope

This standard specifies embeddable and encapsulating markup syntaxes for design intellectual property encryption and rights management, together with recommendations for integration with design specification formats described in other standards. It also recommends use models for interoperable tool and hardware flows, which will include selecting encryption and encoding algorithms and encryption key management. The recommendation includes a description of the trust model assumed in the recommended use models. This standard does not specifically include any consideration of digitally encoded entertainment media. In the context of this document, the term *IP* will be used to mean *electronic design intellectual property*.

*Electronic design intellectual property* is a term used in the electronic design community. It refers to a reusable collection of design specifications that represent the behavior, properties, and/or representation of the design in various media. Examples of these collections include, but are not limited to, the following:

- A unit of electronic system design
- A design verification and analysis scheme (e.g., test bench)
- A netlist indicating elements and the interconnection thereof to implement a function
- A set of fabrication instructions
- A physical layout design or chip layout
- A design intent specification