



IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture

IEEE Computer Society

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Test Technology Standards Committee
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IEEE Computer Society

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Abstract: This specification describes circuitry that may be added to an integrated circuit to provide access to on-chip Test Access Ports (TAPs) specified by IEEE Std 1149.1™-2001. The circuitry uses IEEE 1149.1-2001 as its foundation, providing complete backward compatibility, while aggressively adding features to support test and applications debug. It defines six classes of 1149.7 Test Access Ports (TAP.7s), T0–T5, with each class providing incremental capability, building on that of the lower level classes. Class T0 provides the behavior specified by 1149.1 from startup when there are multiple on-chip TAPs. Class T1 adds common debug functions and features to minimize power consumption. Class T2 adds operating modes that maximize scan performance. It also provides an optional hot-connection capability to prevent system corruption when a connection is made to a powered system. Class T3 supports operation in either a four-wire Series or Star Scan Topology. Class T4 provides for communication with either a two-pin or four-pin interface. The two-pin operation serializes 1149.1 transactions and provides for higher Test Clock rates. Class T5 adds the ability to perform data transfers concurrent with scan, supports utilization of functions other than scan, and provides control of TAP.7 pins to custom debug technologies in a manner that ensures current and future interoperability.

Keywords: 1149.1, 1149.7, 2-pin, 2-wire, 4-pin, 4-wire, Advanced Protocol, Advanced Protocol Unit, APU, Background Data Transfer, background data transport, BDX, boundary scan, BSD, BSDL, BSDL.1, BSDL.7, BYPASS, Capture-IR, CDX, Chip-Level TAP Controller, Class T0, Class T1, Class T2, Class T3, Class T4, Class T5, CLTAPC, compact JTAG, compliant behavior, compliant operation, control level, controller address, Controller ID, Controller Identification Number, CP, Custom Data Transfer, custom data transport, Data Register, debug interface, debug logic, debug and test interface, DOT1, DOT7, DTI, DTS, DTT, Debug Test System, debug test target, Escape, EOT, EPU, extended operation, Extended Protocol, EXTEST, HSDL, HSDL.7, IDCODE, Instruction Register, JScan, JScan0, JScan1, JScan2, JScan3, JTAG, MScan, MTCP, Multi-TAP Control Path, narrow Star Scan Topology, nTRST, nTRST_PD, optimized scan, OScan, OScan0, OScan1, OScan2, OScan3, OScan4, OScan5, OScan6, OScan7, 1149.1, 1149.7, Pause-DR, Pause-IR, PC0, PC1, RSU, Reset and selection unit, RTI, Run-Test/Idle, scan, scan DR, scan format, scan IR, Scan Packet, scan path, scan performance, scan protocol, scan topology, series, Series Branch, Series Scan, Series Scan Topology, Series-Equivalent Scan, Series Topology, Shift-DR, Shift-IR, SiP, Star Scan, Star Scan Topology, Star Topology, Star-2, Star-2 Branch, Star-2 Scan, Star-2 Scan Topology, Star-4, Star-4 Branch, Star-4 Scan, Star-4 Scan Topology, SP, SScan, SScan0, SScan1, SScan2, SScan3, stall, SSD, Scan Selection Directive, Standard Protocol, Star Scan, STL, System Test Logic, TAP, TAP controller, TAP controller address, TAP selection, TAP.1, TAP.7, TAP.7, TAPC, TCA, TCKC, TDI, TDIC, TDOC, TDOE, Test Access Port, test and debug, Test-Logic-Reset, TLR, TMSC, Transport Packet, T0, T0 TAP.7, T1, T1 TAP.7, T2, T2 TAP.7, T3, T3 TAP.7, T4, T4 TAP.7, T4(N), T4(N) TAP.7, T4(W), T4(W) TAP.7, T5, T5 TAP.7, T5(N), T5(N) TAP.7, T5(W), T5(W) TAP.7, TP, Update-DR, Update-IR, ZEP, zero bit scan

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Introduction

This introduction is not part of IEEE Std 1149.7-2009, IEEE Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture.

This standard defines a debug and Test Access Port that provides both compatibility with IEEE Std 1149.1™-2001^a and operation with as few as two pins. It complements IEEE Std 1149.1-2001 and is not intended to replace it. The facilities defined by the standard seek to provide a cost-effective debug and test interface solution supporting the debug and test of applications. The standard supports the needs for application debug of products with complex digital circuitry, applications software, and one or more central processing units (CPUs). The interface also provides a means to instrument these applications concurrent with scan transactions associated with the underlying IEEE 1149.1 foundation.

The process of developing this standard began in 2004 when the Mobile Industry Processor Interface (MIPI) Alliance Test and Debug Working Group was formed. During 2004, a standard that addressed the needs of both test and debug was described and requirements were gathered. The emphasis was on creating an interface that allowed standardization of access to debug and test capabilities on-chip while at the same time addressing the needs of applications developers sharing an integrated circuit Test Access Port with test uses. This interface also targeted making chips exhibit the behavior behavior specified by IEEE Std 1149.1-2001 when multiple Test Access Ports are deployed on a single chip. It was thought that applications development tools vendors would be a big beneficiary of this interface as common connectors providing access to the debug and test interface would be recommended. It was felt that all of this would best be accomplished with an interface that was compatible with chip intellectual property already utilizing IEEE Std 1149.1-2001.

Once the requirements gathering process was completed in 2004, the Test and Debug Working Group turned its attention to proposals for addressing the above requirements. Both competing and complementary proposals were submitted. The proposals were debated, and one was selected as a basis to move forward in April of 2005. A preliminary specification replaced the proposal and was reviewed inside the MIPI Test and Debug Working Group and by the NEXUS standards body in late 2005. Since both bodies felt the applicability of the specification was well beyond their own objectives, they both recommended using the on-chip portions of those specifications as the basis for an IEEE standard in a joint meeting in December of 2005.

Multiple drafts of the specification were completed and reviewed from 2005 until the standard's approval, with the capability provided by the standard expanded along the way. Revisions in the presentation and number of capabilities took place along the way to the standard's unanimous approval in 2009.

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1. Overview

1.1 Scope

The standard will define a link between IEEE 1149.1 interfaces in Debug and Test Systems (DTS) and IEEE 1149.1 (JTAG) interfaces in Target Systems (TS). The link defined by this standard introduces an additional layer between these legacy interfaces. This layer may be viewed as an adapter that provides new functionality and features while preserving all elements of the original IEEE 1149.1 (JTAG) interfaces. The standard will define the link behavior (including timing characteristics of signals), protocols, and functionality of the adapters deployed within the DTS and TS. The standard will not modify or create inconsistencies with IEEE 1149.1 (JTAG). The standard will define a superset of the IEEE 1149.1 specification and achieve compliance with IEEE Std 1149.1™-2001.¹

1.2 Purpose

The purpose of the standard is to define a debug and test interface that meets an expanding set of challenges facing Debug and Test Systems (many of which have emerged since the inception of the original IEEE Std 1149.1) while preserving the hardware and software investments of the many industries currently using IEEE Std 1149.1-2001.

¹ Information on references can be found in Clause 2.