

IEEE Standard Test Access Port and Boundary-Scan Architecture

Sponsor

Test Technology Standards Committee
of the
IEEE Computer Society

Reaffirmed 27 March 2008

Approved 14 June 2001

IEEE-SA Standards Board

Abstract: Circuitry that may be built into an integrated circuit to assist in the test, maintenance, and support of assembled printed circuit boards is defined. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register, such that the component is able to respond to a minimum set of instructions designed to assist with testing of assembled printed circuit boards. Also, a language is defined that allows rigorous description of the component-specific aspects of such testability features.

Keywords: boundary scan, boundary-scan architecture, Boundary-Scan Description Language, boundary-scan register, BSDL, circuit boards, circuitry, integrated circuit, printed circuit boards, TAP, test, test access port, VHDL, VHSIC Hardware Description Language

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Print: ISBN 0-7381-2944-5 SH94949
PDF: ISBN 0-7381-2945-3 SS94949

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Introduction

(This introduction is not part of IEEE Std 1149.1-2001, Standard Test Access Port and Boundary-Scan Architecture.)

This standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The facilities defined by the standard seek to provide a solution to the problem of testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques. They also provide a means of accessing and controlling design-for-test features built into the digital integrated circuits themselves. Such features might, for example, include internal scan paths and self-test functions as well as other features intended to support service applications in the assembled product.

History of the development of this standard

The process of developing this standard began in 1985, when the Joint European Test Action Group (JETAG) was formed in Europe. During 1986, this group expanded to include members from both Europe and North America and, as a result, was renamed the Joint Test Action Group (JTAG). Between 1986 and 1988, the JTAG Technical Subcommittee developed and published a series of proposals for a standardized form of boundary scan. In 1988, the last of these proposals—JTAG Version 2.0—was referred to the IEEE Testability Bus Standards Committee (P1149) for inclusion in the standard then under development. The Testability Bus Standards Committee accepted this approach. It decided that the JTAG proposal should become the basis of a standard within the Testability Bus family, with the result that the P1149.1 project was initiated. Following these decisions, the JTAG Technical Subcommittee became the core of the IEEE Working Group that developed this standard.

After the initial approval of this standard in February 1990 and its subsequent publication, the Working Group immediately began efforts to develop a supplement for the purpose of correction, clarification, and enhancement. This effort, spurred and guided by interaction between developers and users of the original standard, culminated in IEEE Std 1149.1a-1993, which was approved in June 1993.

The major changes to this standard introduced by IEEE Std 1149.1a-1993 were

- The addition of two optional instructions, *CLAMP* and *HIGHZ*, which standardized the names and specifications of features often implemented as design-specific features
- The addition of an optional facility to switch a component from a mode in which it complies to this standard into one in which it supports another design-for-test approach

Further, starting with a proposal made by Kenneth P. Parker and Stig Oresjo in 1990, an effort was undertaken to develop a language to describe components that conform to this standard. This effort concluded in the approval of IEEE Std 1149.1b-1994 in September 1994.

The major change introduced to this standard by IEEE Std 1149.1b-1994 was the addition of Annex B, which defines the Boundary-Scan Description Language. All other changes were minor and were strictly for clarification.

Changes introduced by this revision

This revision is primarily a housekeeping update, designed to consolidate learning from the first 10 years of the standard's use into the standard document.

The principal changes introduced are

- To reduce the risk of accidental entry into test mode, the requirement that a binary code for the *EXTEST* instruction be {000...0} has been removed and use of this binary code for other instructions that result in entry to test mode has been deprecated [see 8.1.1 e), 8.8.1 h), B.8.11.3 d), and B.8.11.3 e)].
- To increase the flexibility with which instructions may be implemented and merged, the implicitly merged *SAMPLE/PRELOAD* instruction has been redefined as two separate instructions: *SAMPLE* and *PRELOAD*. These instructions can continue to share a single binary code, effectively resulting in a merged *SAMPLE/PRELOAD* instruction, but alternatively, they may now share binary codes with other instructions, provided that no rules for any of the merged instructions are violated [see 8.1.1 g), 8.2.1 b), 8.6, 8.7, B.5.1.2, B.6.3 b), B.8.11.3 f), B.8.11.3 g), B.8.11.3 h), B.8.11.3 i), B.8.11.3 j), and B.8.13.3 a)].
- To enable more efficient implementation of boundary-scan register cells provided at system logic outputs, the source of data to be captured in such cells in response to the *SAMPLE* instruction is now allowed to be at the connected system pin [see 8.6.1 d), 11.6.1 a), 11.6.1 b), B.8.14.4 l), and B.10.2.4.1 b)]. Additionally, three new cell types based on this implementation, **BC_1**, **BC_9**, and **BC_10** have been added to the Standard VHDL Package (see B.5.1.2, B.9, and Table B.3).
- To permit more flexible boundary-scan register cell implementations, sharing of circuitry between the boundary-scan register and other elements of the test and/or system logic has been allowed in limited cases [see 11.2.1 j) and 11.2.1 k)].
- To support more complete description of IC pin drivers with bus keeper circuits, a new value for <disable result> has been defined (**KEEPER**, see B.5.1.2, B.8.14.4 l), and B.8.14.3.7).
- To track the widespread acceptance of BSDL, the language has been made a normative part of the standard and its use for documentation has been mandated (see 13.3.1 c) and Annex B).

Additionally, a number of minor changes were made to correct and clarify the language of the standard [of special note, see 4.8.1 c), 11.7.1 b), B.8.14.4 h), and B.8.14.4 n)].

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Contents

1. Overview.....	1
1.1 Scope.....	1
1.2 Purpose.....	1
1.3 Document outline.....	5
1.4 Conventions	6
2. References.....	6
3. Definitions and Acronyms	6
3.1 Definitions	6
3.2 Acronyms.....	9
4. Test access port (TAP).....	9
4.1 Connections that form the test access port (TAP)	9
4.2 Test clock input (TCK).....	9
4.3 Test mode select input (TMS)	11
4.4 Test data input (TDI).....	11
4.5 Test data output (TDO).....	12
4.6 Test reset input (TRST*)	12
4.7 Interconnection of components compatible with this standard	13
4.8 Subordination of this standard within a higher-level test strategy.....	15
5. Test logic architecture.....	16
5.1 Test logic design	17
5.2 Test logic realization.....	17
6. The TAP controller	18
6.1 TAP controller state diagram	18
6.2 TAP controller operation	24
6.3 TAP controller initialization	30
7. The instruction register	33
7.1 Design and construction of the instruction register	33
7.2 Instruction register operation	34
8. Instructions.....	36
8.1 Response of the test logic to instructions.....	36
8.2 Public instructions.....	37
8.3 Private instructions	38
8.4 The <i>BYPASS</i> instruction.....	38
8.5 Boundary-scan register instructions.....	39
8.6 The <i>SAMPLE</i> instruction	41
8.7 The <i>PRELOAD</i> instruction	43
8.8 The <i>EXTEST</i> instruction	45

8.9	The <i>INTEST</i> instruction	48
8.10	The <i>RUNBIST</i> instruction	53
8.11	The <i>CLAMP</i> instruction	56
8.12	Device identification register instructions	57
8.13	The <i>IDCODE</i> instruction	58
8.14	The <i>USERCODE</i> instruction	58
8.15	The <i>HIGHZ</i> instruction	59
9.	Test data registers	61
9.1	Provision of test data registers	61
9.2	Design and construction of test data registers	63
9.3	Test data register operation	64
10.	The bypass register	66
10.1	Design and operation of the bypass register	66
11.	The boundary-scan register	67
11.1	Introduction	68
11.2	Register design	72
11.3	Register operation	74
11.4	General rules regarding cell provision	76
11.5	Provision and operation of cells at system logic inputs	79
11.6	Provision and operation of cells at system logic outputs	87
11.7	Provision and operation of cells at bidirectional system logic pins	102
11.8	Redundant cells	108
11.9	Special cases	109
12.	The device identification register	111
12.1	Design and operation of the device identification register	112
12.2	Manufacturer identity code	114
12.3	Part number code	115
12.4	Version code	115
13.	Conformance and documentation requirements	115
13.1	Claiming conformance to this standard	115
13.2	Prime and second source components	117
13.3	Documentation requirements	117
	Annex A (informative) An example implementation using level-sensitive design techniques	120
	Annex B (normative) Boundary-scan description language	129

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IEEE Standard Test Access Port and Boundary-Scan Architecture

1. Overview

1.1 Scope

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to

- testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate;
- testing the integrated circuit itself; and
- observing or modifying circuit activity during the component's normal operation.

The test logic consists of a boundary-scan register and other building blocks and is accessed through a Test Access Port (TAP).

1.2 Purpose

1.2.1 An overview of the operation of IEEE Std 1149.1

This subclause provides a general overview of the operation of a component compatible with this standard and provides a background to the detailed discussion in later subclauses.

The circuitry defined by this standard allows test instructions and associated test data to be fed into a component and, subsequently, allows the results of execution of such instructions to be read out. All information (instructions, test data, and test results) is communicated in a serial format.

The sequence of operations would be controlled by a bus master, which could be either an automatic test equipment (ATE) or a component that interfaces to a higher-level test bus as a part of a complete system maintenance architecture. Control is achieved through signals applied to the Test Mode Select (TMS) and Test Clock (TCK) inputs of the various components connected to the bus master. Starting from an initial state in which the test circuitry defined by this standard is inactive, a typical sequence of operations would be as follows.

The first steps would be, in general, to load serially into the component the instruction binary code for the particular operation to be performed. The test logic defined by this standard is designed such that the serial movement of instruction information is not apparent to those circuit blocks whose operation is controlled by the instruction. The instruction applied to these blocks changes only on completion of the shifting (instruction load) process.

Once the instruction has been loaded, the selected test circuitry is configured to respond. In some cases, however, it is necessary to load data into the selected test circuitry before a meaningful response can be made. Such data is loaded into the component serially in a manner analogous to the process used previously to load the instruction. Note that the movement of test data has no effect on the instruction present in the test circuitry.

After execution of the test instruction, based where necessary on supplied data, the results of the test can be examined by shifting data out of the component to or through the bus master.

Note that in cases where the same test operation is to be repeated but with different data, new test data can be shifted into the component while the test results are shifted out. There is no need for the instruction to be reloaded.

Operation of the test circuitry may proceed by loading and executing several further instructions in a manner similar to that described and would conclude by returning the test circuitry and, where required, on-chip system circuitry to its initial state.

1.2.2 The use of IEEE Std 1149.1 to test an assembled product

This subclause outlines the use of the boundary-scan circuitry defined by this standard during the process of testing an assembled product such as a printed circuit board.

The test problem for any product constructed from a collection of components can be decomposed into three goals:

- a) To confirm that each component performs its required function;
- b) To confirm that the components are interconnected in the correct manner; and
- c) To confirm that the components within the product interact correctly and that the product performs its intended function.

This approach can be applied to a board constructed from integrated circuits, to a system constructed from printed circuit boards, or to a complex integrated circuit constructed from a set of simpler functional modules. To simplify the discussion, this description henceforth will concentrate on the case of an assembled printed circuit board constructed from a collection of digital integrated circuits.

At the board level, goal a) and goal b) typically are achieved by using in-circuit test techniques; for goal c), a functional test is required. However, in-circuit test techniques have significant limitations when viewed against evolving surface-mount interconnection technology, for example, the difficulty of making reliable contact to miniaturized features of the printed circuit board using a bed-of-nails fixture. How, then, might the above three test goals be achieved if test access becomes limited to the normal circuit connections, plus a relatively small number of special-purpose test connections?

Considering goal a), it is clear that the vendor of an integrated circuit used in the board-level design will have an established test methodology for that component. The components could be tested on a proprietary ATE system or by using a self-test procedure embedded in the design. Information on the test methodology adopted is typically not available to the component purchaser. Even where self-test modes of operation are known to exist, they may not be documented and therefore are not available to the component user. Alternative sources of test data for the board test engineer may be the component test libraries supplied with

in-circuit test systems or the test programs developed by component users for incoming inspection of delivered devices.

Wherever the test data for a component originates, the next step is to use it once the component has been assembled onto the printed circuit board. If access is limited to the normal connections of the assembled circuit, this task may be far from simple. This is particularly true if the surrounding components are complex or if the board designer has tied some of the components' connections to fixed logic levels or has left component pins unconnected. Normally, it will not be possible to test the component in the same way that it was tested in isolation unless an in-circuit test is achievable.

To ensure that built-in test facilities can be used or that preexisting test patterns can be applied, a framework is needed that can be used to convey test data to or from the boundaries of individual components so that they can be tested as if they were freestanding. This framework will also allow access to and control of built-in test facilities of components. Boundary scan coupled with a test access bus provides such a framework.

The objective of this standard is to define a boundary-scan architecture that can be adopted as a standard feature of integrated circuit designs, thus allowing the required test framework to be created on assembled printed circuit boards and other products.

1.2.3 What is boundary scan?

The boundary-scan technique involves the inclusion of a shift-register stage (contained in a boundary-scan register cell) adjacent to each component pin so that signals at component boundaries can be controlled and observed using scan testing principles.

Figure 1-1 illustrates an example implementation for a boundary-scan register cell that could be used for an input or output connection to an integrated circuit. Dependent on the control signals applied to the multiplexers, data can be either loaded into the scan register from the Signal-in port (e.g., the input pin) or driven from the register through the Signal-out port of the cell (e.g., into the core of the component design). As will be discussed in detail in Clause 11, the second flip-flop (controlled by input Clock B) is provided to ensure that the signals driven out of the cell in the latter case are held while new data is shifted into the cell using input Clock A. This flip-flop is not required in all cases but is included in Figure 1-1 to simplify the discussion.

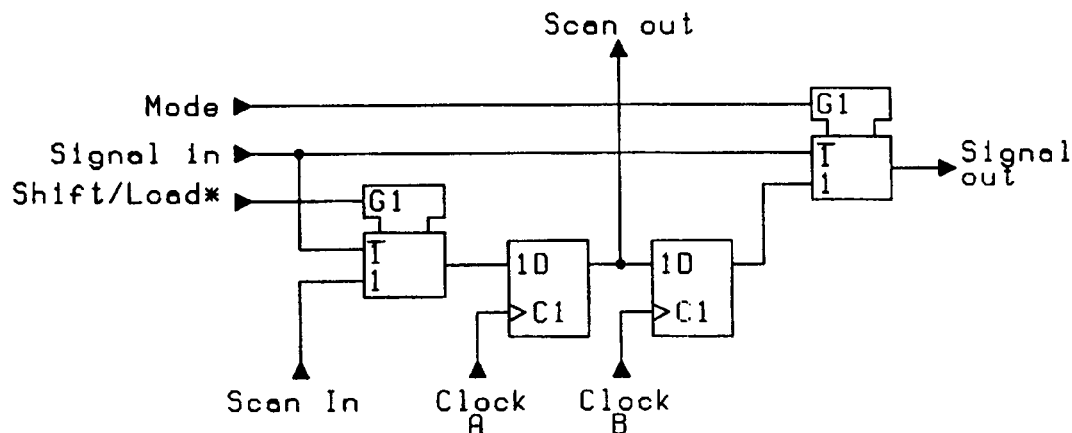


Figure 1-1—A boundary-scan register cell

The boundary-scan register cells for the pins of a component are interconnected to form a shift-register chain around the border of the design, and this path is provided with serial input and output connections and