



IEEE Standard VHDL Language Reference Manual

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(Revision of
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Abstract: VHSIC Hardware Description Language (VHDL) is defined. VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. Its primary audiences are the implementors of tools supporting the language and the advanced users of the language.

Keywords: computer languages, electronic systems, hardware, hardware design, VHDL

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Introduction

This introduction is not part of IEEE Std 1076-2008, IEEE Standard VHDL Language Reference Manual.

The VHSIC Hardware Description Language (VHDL) is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware.

This document, IEEE Std 1076-2008, is a revision of IEEE Std 1076-2002 as amended by IEEE Std 1076c™-2007. Initial work on gathering requirements and developing language extensions was undertaken by the IEEE VHDL Analysis and Standardization Group (VASG), otherwise known as the 1076 Working Group. Subsequently, Accellera^a sponsored an effort to complete that work and draft a revised Language Reference Manual. That draft was returned to IEEE for final revision and approval, resulting in this document and the associated machine-readable files. This revision incorporates numerous enhancements, both major and minor, to previously existing language features and several new language features. The changes are summarized in Annex E. In addition, several VHDL library packages that were previously defined in separate standards are now defined in this standard, ensuring that they are treated as integral parts of the language. Finally, this revision incorporates the IEEE Property Specification Language (PSL) as part of VHDL. The combination of these changes significantly improves VHDL as a language for specification, design, and verification of complex electronic systems.

The maintenance of the VHDL language standard is an ongoing process. The chair of the VHDL Analysis and Standardization Group extends his gratitude to all who have participated in this revision, both in the IEEE committees and the Accellera effort, and encourages the participation of all interested parties in future language revisions.^b

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Contents

1.	Overview of this standard	1
1.1	Scope.....	1
1.2	Purpose.....	1
1.3	Structure and terminology of this standard.....	2
2.	Normative references	5
3.	Design entities and configurations.....	7
3.1	General.....	7
3.2	Entity declarations	7
3.3	Architecture bodies	10
3.4	Configuration declarations.....	13
4.	Subprograms and packages.....	19
4.1	General.....	19
4.2	Subprogram declarations	19
4.3	Subprogram bodies	23
4.4	Subprogram instantiation declarations.....	26
4.5	Subprogram overloading.....	26
4.6	Resolution functions	29
4.7	Package declarations.....	30
4.8	Package bodies.....	31
4.9	Package instantiation declarations	33
4.10	Conformance rules.....	34
5.	Types.....	35
5.1	General.....	35
5.2	Scalar types	36
5.3	Composite types.....	44
5.4	Access types.....	53
5.5	File types.....	55
5.6	Protected types	58
5.7	String representations	61
6.	Declarations	63
6.1	General.....	63
6.2	Type declarations	64
6.3	Subtype declarations	64
6.4	Objects	66
6.5	Interface declarations	73
6.6	Alias declarations.....	89
6.7	Attribute declarations.....	92
6.8	Component declarations	93
6.9	Group template declarations	93
6.10	Group declarations	93
6.11	PSL clock declarations.....	94

7.	Specifications.....	95
7.1	General.....	95
7.2	Attribute specification.....	95
7.3	Configuration specification.....	98
7.4	Disconnection specification.....	103
8.	Names	107
8.1	General.....	107
8.2	Simple names.....	108
8.3	Selected names.....	109
8.4	Indexed names	111
8.5	Slice names	112
8.6	Attribute names.....	112
8.7	External names.....	113
9.	Expressions	117
9.1	General.....	117
9.2	Operators.....	118
9.3	Operands	131
9.4	Static expressions.....	139
9.5	Universal expressions	142
10.	Sequential statements.....	145
10.1	General.....	145
10.2	Wait statement	145
10.3	Assertion statement.....	147
10.4	Report statement	148
10.5	Signal assignment statement.....	149
10.6	Variable assignment statement.....	160
10.7	Procedure call statement.....	163
10.8	If statement	164
10.9	Case statement	164
10.10	Loop statement.....	166
10.11	Next statement.....	167
10.12	Exit statement.....	167
10.13	Return statement.....	168
10.14	Null statement.....	168
11.	Concurrent statements.....	169
11.1	General.....	169
11.2	Block statement.....	169
11.3	Process statement.....	170
11.4	Concurrent procedure call statements.....	172
11.5	Concurrent assertion statements	173
11.6	Concurrent signal assignment statements	174
11.7	Component instantiation statements	176
11.8	Generate statements	182

12.	Scope and visibility.....	185
	12.1 Declarative region.....	185
	12.2 Scope of declarations.....	185
	12.3 Visibility.....	187
	12.4 Use clauses.....	191
	12.5 The context of overload resolution.....	192
13.	Design units and their analysis.....	195
	13.1 Design units.....	195
	13.2 Design libraries.....	195
	13.3 Context declarations.....	197
	13.4 Context clauses.....	197
	13.5 Order of analysis.....	198
14.	Elaboration and execution.....	199
	14.1 General.....	199
	14.2 Elaboration of a design hierarchy.....	199
	14.3 Elaboration of a block, package, or subprogram header.....	202
	14.4 Elaboration of a declarative part.....	205
	14.5 Elaboration of a statement part.....	210
	14.6 Dynamic elaboration.....	213
	14.7 Execution of a model.....	214
15.	Lexical elements.....	225
	15.1 General.....	225
	15.2 Character set.....	225
	15.3 Lexical elements, separators, and delimiters.....	227
	15.4 Identifiers.....	229
	15.5 Abstract literals.....	230
	15.6 Character literals.....	231
	15.7 String literals.....	231
	15.8 Bit string literals.....	232
	15.9 Comments.....	234
	15.10Reserved words.....	235
	15.11Tool directives.....	237
16.	Predefined language environment.....	239
	16.1 General.....	239
	16.2 Predefined attributes.....	239
	16.3 Package STANDARD.....	254
	16.4 Package TEXTIO.....	268
	16.5 Standard environment package.....	274
	16.6 Standard mathematical packages.....	275
	16.7 Standard multivalued logic package.....	276
	16.8 Standard synthesis packages.....	277
	16.9 Standard synthesis context declarations.....	283
	16.10Fixed-point package.....	283
	16.11Floating-point package.....	284

17.	VHDL Procedural Interface overview	285
	17.1 General.....	285
	17.2 Organization of the interface	285
	17.3 Capability sets.....	286
	17.4 Handles	288
18.	VHPI access functions	291
	18.1 General.....	291
	18.2 Information access functions	291
	18.3 Property access functions.....	293
	18.4 Access by name function	294
19.	VHPI information model	295
	19.1 General.....	295
	19.2 Formal notation.....	295
	19.3 Class inheritance hierarchy	296
	19.4 Name properties	297
	19.5 The stdUninstantiated package	310
	19.6 The stdHierarchy package	313
	19.7 The stdTypes package.....	320
	19.8 The stdExpr package.....	322
	19.9 The stdSpec package.....	325
	19.10The stdSubprograms package	327
	19.11The stdStmts package	329
	19.12The stdConnectivity package.....	335
	19.13The stdCallbacks package.....	340
	19.14The stdEngine package	340
	19.15The stdForeign package	341
	19.16The stdMeta package	341
	19.17The stdTool package.....	343
	19.18Application contexts	344
20.	VHPI tool execution	345
	20.1 General.....	345
	20.2 Registration phase.....	345
	20.3 Analysis phase	351
	20.4 Elaboration phase.....	351
	20.5 Initialization phase	353
	20.6 Simulation phase.....	353
	20.7 Save phase.....	353
	20.8 Restart phase	354
	20.9 Reset phase	354
	20.10Termination phase.....	355
21.	VHPI callbacks	357
	21.1 General.....	357
	21.2 Callback functions	357
	21.3 Callback reasons	359

22.	VHPI value access and update	371
	22.1 General	371
	22.2 Value structures and types	371
	22.3 Reading object values	374
	22.4 Formatting values	375
	22.5 Updating object values.....	377
	22.6 Scheduling transactions on drivers	381
23.	VHPI function reference	385
	23.1 General.....	385
	23.2 vhpi_assert	385
	23.3 vhpi_check_error	386
	23.4 vhpi_compare_handles	388
	23.5 vhpi_control	389
	23.6 vhpi_create.....	390
	23.7 vhpi_disable_cb	392
	23.8 vhpi_enable_cb	393
	23.9 vhpi_format_value	394
	23.10vhpi_get	396
	23.11vhpi_get_cb_info	396
	23.12vhpi_get_data.....	397
	23.13vhpi_get_foreignf_info	399
	23.14vhpi_get_next_time	400
	23.15vhpi_get_phys.....	401
	23.16vhpi_get_real	402
	23.17vhpi_get_str	402
	23.18vhpi_get_time	403
	23.19vhpi_get_value.....	404
	23.20vhpi_handle.....	405
	23.21vhpi_handle_by_index.....	406
	23.22vhpi_handle_by_name	408
	23.23vhpi_is_printable	410
	23.24vhpi_iterator.....	411
	23.25vhpi_printf	412
	23.26vhpi_protected_call.....	413
	23.27vhpi_put_data.....	415
	23.28vhpi_put_value.....	417
	23.29vhpi_register_cb.....	418
	23.30vhpi_register_foreignf	419
	23.31vhpi_release_handle.....	421
	23.32vhpi_remove_cb.....	422
	23.33vhpi_scan	422
	23.34vhpi_schedule_transaction.....	423
	23.35vhpi_vprintf	426
24.	Standard tool directives	429
	24.1 Protect tool directives	429
	Annex A (informative) Description of accompanying files	447
	Annex B (normative) VHPI header file	451

Annex C (informative) Syntax summary	477
Annex D (informative) Potentially nonportable constructs	501
Annex E (informative) Changes from IEEE Std 1076-2002	503
Annex F (informative) Features under consideration for removal	511
Annex G (informative) Guide to use of standard packages	513
Annex H (informative) Guide to use of protect directives	551
Annex I (informative) Glossary	557
Annex J (informative) Bibliography	585
Index	587

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1. Overview

1.1 Scope

This standard revises and enhances the VHDL language reference manual (LRM) by including a standard C language interface specification; specifications from previously separate, but related, standards IEEE Std 1164TM-1993 [B16],¹ IEEE Std 1076.2TM-1996 [B11], and IEEE Std 1076.3TM-1997 [B12]; and general language enhancements in the areas of design and verification of electronic systems.

1.2 Purpose

The VHDL language was defined for use in the design and documentation of electronics systems. It is revised to incorporate capabilities that improve the language’s usefulness for its intended purpose as well as extend it to address design verification methodologies that have developed in industry. These new design and verification capabilities are required to ensure VHDL remains relevant and valuable for use in electronic systems design and verification. Incorporation of previously separate, but related standards, simplifies the maintenance of the specifications.

¹The numbers in brackets correspond to those of the bibliography in Annex J.