IEC 63505

Edition 1.0 2025-04

INTERNATIONAL STANDARD

Guidelines for measuring the threshold voltage (V_{th}) of SiC MOSFETs

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INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

ICS 31.080.30

ISBN 978-2-8327-0325-0

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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[1] Numbers in square brackets refer to the Bibliography.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2885/FDIS	47/2908/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

The structure and editorial rules used in this publication reflect the practice of the organization which submitted it.

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The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

INTRODUCTION

This document is intended for use in the SiC power semiconductor and related power electronic industries and provides guidelines for measuring the threshold voltage (V_T) of SiC power devices.

Threshold voltage (V_T) is a key parameter in the evaluation of changes in the characteristics of physical stimulus such as voltage and/or temperature stress. Without accurately measuring threshold voltage, it is not possible to monitor how device characteristics are changed by the stress applied to a device.

SiC/SiO_2 interface of Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is more complex than the Si/SiO_2 interface, which requires careful handling of traps in the device with regard to the change monitoring of characteristics.

The test methods provided in this document can be used as a guideline for measuring threshold voltage of SiC power device, focused on N-channel vertical structure MOSFET technologies. These three test methods can be applied for datasheet, process control, technology development, final tests and other usage.

GUIDELINES FOR MEASURING THE THRESHOLD VOLTAGE (V_T) OF SIC MOSFETS

1 Scope

This document gives guidance on V_T measurement methods and conditioning prior to V_T testing in SiC power MOSFETs to reduce or eliminate the effect of the aforementioned hysteresis. The method is applicable for PBTI testing, NBTI and threshold voltage changes caused by switching events are excluded from the scope.

SiC MOSFETs have threshold voltage hysteresis caused by transient trap effects, which impacts the evaluation of the actual the V_T shift caused by stress tests such as bias temperature instabilities (BTI) [2].

The test methods can be applied to the following:

a) N-channel SiC MOSFET (vertical structure);
b) the above in wafer and package levels.

2 Normative references

There are no normative references in this document.

3 Terms, definitions, and letter symbols

3.1 Terms and definitions

No terms and definitions are listed in this document.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.2 Letter symbols

DUT	Device Under Test
NBTI	Negative-Bias Temperature Instability
PBTI	Positive- Bias Temperature Instability
V_{DD}	Supply voltage
V_{DS}	Drain to Source Voltage of DUT
V_{GS}	Gate to Source Voltage of DUT
V_T	Threshold voltage of DUT
V_T^{UP}	Threshold voltage of DUT taken by upward sweep
V_T^{DOWN}	Threshold voltage of DUT taken by downward sweep
$V_{T\ (GDS)}$	Threshold voltage of DUT measured by test circuit where gate and drain are shorted
I_{DS}	Drain-Source current