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Integrated circuits – Three dimensional integrated circuits – Part 3: Model and measurement conditions of through-silicon via

Circuits intégrés – Circuits intégrés tridimensionnels – Partie 3: Modèle et conditions de mesure des trous de liaison à travers le silicium

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

FOREWORD

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The text of this International Standard is based on the following documents:

FDIS	Report on voting
47A/1057/FDIS	47A/1063/RVD

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 63011 series, under the general title *Integrated circuits – Three dimensional integrated circuits*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

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INTRODUCTION

The embedded system implementation such as digital consumer and mobile devices is a history of functional integration and power reduction for faster and smaller. At the beginning, the embedded system was developed by various digital ASIC chips to implement required functions. They were then integrated on one chip as a system on chip (SoC), which includes application processor and peripheral I/F logic, such as PCIe, SATA, USB, and DDRx memory controller. Because required performance and image resolution is growing, SoC has embedded many functions through adopting advanced semiconductor technology.

Since advanced semiconductor technology is complicated and its development cost is higher, the application is limited to use only for a few products. Those SoC's cost is not appropriate for all embedded systems. Multi-chip implementation is a way to solve this issue. It implements very large logic gate on the separated SoC and ASIC logic chips, connecting each other. This multi-chip interconnection technique provides also implementation of heterogeneous technology VLSI chips.

This document is focused to interconnect methodology to implement multi-chip VLSI for three-dimensional integrated circuit. Thanks to through-silicon via (TSV) and micro bump interconnect technology; the wire number between VLSI can be tremendously wider. It also allows to connect chips with on-chip bus interconnection, which has several thousand signal connections.

INTEGRATED CIRCUITS – THREE DIMENSIONAL INTEGRATED CIRCUITS –

Part 3: Model and measurement conditions of through-silicon via

1 Scope

This part of IEC 63011 specifies a reference model of through-silicon via (TSV) electrical characteristics required for an interface design in three dimensional integrated circuit (3-D IC) to transmit and receive digital data and measurement conditions for resistance and capacitance to specify TSV characteristics in 3-D IC.

3-D IC specifications covered by this document are the following:

- application: digital consumer and mobile;
- operating voltage: 0,1 V to 5,0 V,
- operating frequency: less than 2,0 GHz.

This document does not describe the equipment for the measurement. Figure 1 describes a typical case of multi-chip interconnect system discussed in this document.

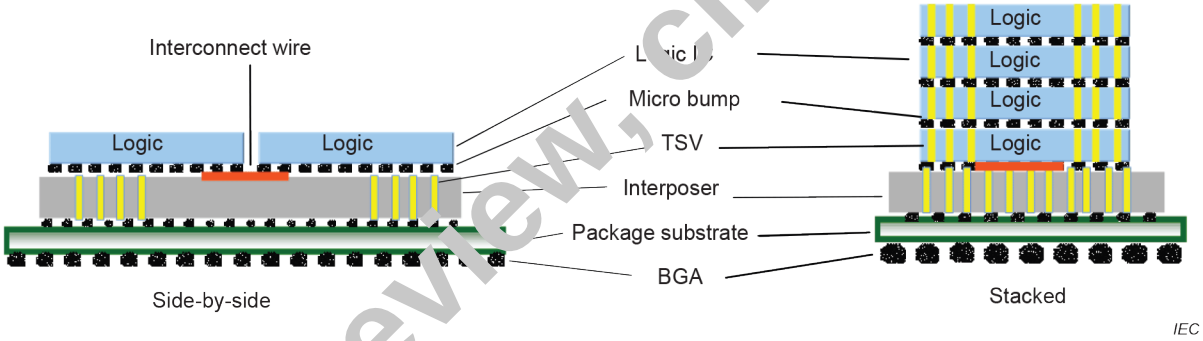

Figure 1 – Reference of a multi-chip interconnect system

Power devices, RF devices and micro-electromechanical systems (MEMS) are not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63011-1, *Integrated circuits – Three dimensional integrated circuits – Part 1: Terminology*