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SystemVerilog –
Part 2: Universal Verification Methodology Language Reference Manual

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Contents

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IEEE Standard for Universal Verification Methodology Language Reference Manual

Developed by the

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 4 June 2020

IEEE SA Standards Board

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Accellera Systems Initiative—*The Universal Verification Methodology (UVM) Pre-IEEE Class Reference*.

Abstract: The Universal Verification Methodology (UVM) that can improve interoperability, reduce the cost of using intellectual property (IP) for new projects or electronic design automation (EDA) tools, and make it easier to reuse verification components is provided. Overall, using this standard will lower verification costs and improve design quality throughout the industry. The primary audiences for this standard are the implementors of the UVM base class library, the implementors of tools supporting the UVM base class library, and the users of the UVM base class library.

Keywords: agent, blocking, callback, class, component, consumer, driver, event, export, factory, function, generator, IEEE 1800.2™, member, method, monitor, non-blocking, phase, port, register, resource, sequence, sequencer, transaction-level modeling, verification methodology

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Introduction

This introduction is not part of IEEE Std 1800.2™-2020, IEEE Standard for Universal Verification Methodology Language Reference Manual.

Verification has evolved into a complex project that often spans internal and external teams, but the discontinuity associated with multiple, incompatible methodologies among those teams can limit productivity. The Universal Verification Methodology (UVM) Language Reference Manual (LRM) addresses verification complexity and interoperability within companies and throughout the electronics industry for both novice and advanced teams while also providing consistency. While UVM is revolutionary, being the first verification methodology to be standardized, it is also evolutionary, as it is built on the Open Verification Methodology (OVM), which combined the Advanced Verification Methodology (AVM) with the Universal Reuse Methodology (URM) and concepts from the e Reuse Methodology (eRM). Furthermore, UVM also infuses concepts and code from the Verification Methodology Manual (VMM), plus the collective experience and knowledge of the over 300 members of the Accellera UVM Working Group to help standardize verification methodology. Finally, the transaction-level modeling (TLM) facilities in UVM are based on what was developed by Open SystemC Initiative (OSCI) for SystemC, though they are not an exact replication or re-implementation of the SystemC TLM library.

IEEE Standard for Universal Verification Methodology Language Reference Manual

1. Overview

1.1 Scope

This standard establishes the Universal Verification Methodology (UVM), a set of application programming interfaces (APIs) that defines a base class library (BCL) definition used to develop modular, scalable, and reusable components for functional verification environments. The APIs and BCL are based on the IEEE standard for SystemVerilog, IEEE Std 1800™.[1]

1.2 Purpose

Verification components and environments are currently created in different forms, making interoperability among verification tools and/or geographically dispersed design environments both time consuming to develop and error prone. The results of the UVM standardization effort will improve interoperability and reduce the cost of repurchasing and rewriting intellectual property (IP) for each new project or electronic design automation (EDA) tool, as well as make it easier to reuse verification components. Overall, the UVM standardization effort will lower verification costs and improve design quality throughout the industry.

1.3 Word usage

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*).[2, 3]

The word *should* indicates that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required (*should* equals *is recommended that*).

The word *may* is used to indicate a course of action permissible within the limits of the standard (*may* equals *is permitted to*).

The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

[1] Information on references can be found in Clause 2.

[2] The use of the word *must* is deprecated and cannot be used when stating mandatory requirements, *must* is used only to describe unavoidable situations.

[3] The use of *will* is deprecated and cannot be used when stating mandatory requirements, *will* is only used in statements of fact.