INTERNATIONAL STANDARD

IEC 62142

First edition
2005-06

IEEE 1364.1™

Verilog® register transfer level synthesis

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

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International Standard IEC/IEEE 62142 has been processed through IEC technical committee 93: Design automation.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1364.1 (2002)	93/213/FDIS	93/218/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

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The committee has decided that the contents of this publication will remain unchanged until 2007.

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IEEE Standard for Verilog® Register Transfer Level Synthesis

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 10 December 2002

IEEE-SA Standards Board

Abstract: Standard syntax and semantics for Verilog® HDL-based RTL synthesis are described in this standard.
Keywords: hardware description language, HDL, RTL, synthesis, Verilog®

IEEE Introduction

This standard describes a standard syntax and semantics for Verilog® HDL-based RTL synthesis. It defines the subset of IEEE Std 1364-2001 (Verilog HDL) that is suitable for RTL synthesis and defines the semantics of that subset for the synthesis domain.

The purpose of this standard is to define a syntax and semantics that can be used in common by all compliant RTL synthesis tools to achieve uniformity of results in a similar manner to which simulation and analysis tools use IEEE Std 1364-2001. This will allow users of synthesis tools to produce well-defined designs whose functional characteristics are independent of a particular synthesis implementation by making their designs compliant with this standard.

The standard is intended for use by logic designers and electronic engineers.

Initial work on this standard started as a RTL synthesis subset working group under Open Verilog International (OVI). After OVI approved of the draft 1.0 with an overwhelming affirmative response, an IEEE Project Authorization Request (PAR) was obtained in July 1998 to clear its way for IEEE standardization. Most of the members of the original group continued to be part of the Pilot Group under P1364.1 to lead the technical work. The active members at the time of OVI draft 1.0 publication were as follows:

J. Bhasker, *Chair*

Victor Berman	Don Hejna	Doug Smith
David Bishop	Mike Quayle	Yatin Trivedi
Vassilios Gerousis	Ambar Sarkar	Rohit Vora

An approved draft D1.4 was ready by April 1999, thanks very much to the efforts of the following task leaders:

David Bishop (Web Admin.)	Don Hejna (Syntax)	Doug Smith (Pragmas)
Ken Coffman (Semantics)		Yatin Trivedi (Editor)

When the working group was ready to initiate the standardization process, it was decided to postpone the process for the following reasons:

a) The synthesis subset draft was based on Verilog IEEE Std 1364-1995.

b) A new updated Verilog language was imminent.

c) The new Verilog language contained many new synthesizable constructs.

It wasn't until early 2001 that Verilog IEEE Std 1364-2001 was finalized. The working group restarted their work by first looking at the synthesizability aspects of the new features in the language. Thereafter, RAM/ROM modeling features and new attributes syntax were introduced into the draft standard.

Many individuals from many different organizations participated directly or indirectly in the standardization process. A majority of the working group meetings were held via teleconferences with continued discussions on the working group reflector.

VERILOG® REGISTER TRANSFER LEVEL SYNTHESIS

1. Overview

1.1 Scope

This standard defines a set of modeling rules for writing Verilog® HDL descriptions for synthesis. Adherence to these rules guarantees the interoperability of Verilog HDL descriptions between register-transfer level synthesis tools that comply to this standard. The standard defines how the semantics of Verilog HDL are used, for example, to describe level- and edge-sensitive logic. It also describes the syntax of the language with reference to what shall be supported and what shall not be supported for interoperability.

Use of this standard will enhance the portability of Verilog-HDL-based designs across synthesis tools conforming to this standard. In addition, it will minimize the potential for functional mismatch that may occur between the RTL model and the synthesized netlist.

1.2 Compliance to this standard

1.2.1 Model compliance

A Verilog HDL model shall be considered compliant to this standard if the model:

a) uses only constructs described as supported or ignored in this standard, and
b) adheres to the semantics defined in this standard.

1.2.2 Tool compliance

A synthesis tool shall be considered compliant to this standard if it:

a) accepts all models that adhere to the model compliance definition in 1.2.1.
b) supports all pragmas defined in Clause 6.
c) produces a netlist model that has the same functionality as the input model based on the conformance rules of Clause 4.

NOTE—A compliant synthesis tool may have more features than those required by this standard. A synthesis tool may introduce additional guidelines for writing Verilog HDL models that may produce more efficient logic, or other mechanisms for controlling how a particular description is best mapped to a particular library.

1.3 Terminology

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). The word *should* is used to indicate that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*). The word *may* indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

A synthesis tool is said to *accept* a Verilog construct if it allows that construct to be legal input. The construct is said to *interpret* the construct (or to provide an *interpretation* of the construct) by producing logic that represents the construct. A synthesis tool shall not be required to provide an interpretation for every construct that it accepts, but only for those for which an interpretation is specified by this standard.

The Verilog HDL constructs in this standard are categorized as:

— **Supported:** RTL synthesis shall interpret and map the construct to hardware.
— **Ignored:** RTL synthesis shall ignore the construct and shall not map that construct to hardware. Encountering the construct shall not cause synthesis to fail, but may cause a functional mismatch between the RTL model and the synthesized netlist. The mechanism, if any, by which a RTL synthesis notifies the user of such constructs is not defined. It is acceptable for a not supported construct to be part of an ignored construct.
— **Not supported:** RTL synthesis shall not support the construct. An RTL synthesis tool shall fail upon encountering the construct, and the failure mode shall be undefined.

1.4 Conventions

This standard uses the following conventions:

a) The body of the text of this standard uses **boldface** font to denote Verilog reserved words (such as **if**).
b) The text of the Verilog examples and code fragments is represented in a `fixed-width` font.
c) Syntax text that is ~~struck-through~~ refers to syntax that is not supported.
d) Syntax text that is underlined refers to syntax that is ignored.
e) "<" and ">" are used to represent text in one of several different, but specific forms.
f) Any paragraph starting with "NOTE—" is informative and not part of the standard.
g) In the PDF version of this standard, colors are used in Clause 7 and Annex A. Supported reserved words are in red **boldface** font. Blue ~~struck-through~~ are unsupported constructs, and blue underlined are ignored constructs.

1.5 Contents of this standard

A synopsis of the clauses and annexes is presented as a quick reference. There are seven clauses and two annexes. All the clauses are the normative parts of this standard, while all the annexes are the informative part of the standard.

a) **Clause 1—Overview:** This clause discusses the conventions used in this standard and its contents.
b) **Clause 2—References:** This clause contains bibliographic entries pertaining to this standard.
c) **Clause 3—Definitions:** This clause defines various terms used in this standard.
d) **Clause 4—Verification methodology:** This clause describes the guidelines for ensuring functionality matches before and after synthesis.
e) **Clause 5—Modeling hardware elements:** This clause defines the styles for inferring special hardware elements.

f) **Clause 6—Pragmas:** This clause defines the pragmas that are part of this RTL synthesis subset.
g) **Clause 7—Syntax:** This clause describes the syntax of Verilog HDL supported for RTL synthesis.
h) **Annex A—Syntax summary:** This informative annex provides a summary of the syntax supported for synthesis.
i) **Annex B—Functional mismatches:** This informative annex describes some cases where a potential exists for functional mismatch to occur between the RTL model and the synthesized netlist.

1.6 Examples

All examples that appear in this document under *"Example:"* are for the sole purpose of demonstrating the syntax and semantics of Verilog HDL for synthesis. It is not the intent of this clause to demonstrate, recommend, or emphasize coding styles that are more (or less efficient) in generating synthesizable hardware. In addition, it is not the intent of this standard to present examples that represent a compliance test suite or performance benchmark, even though these examples are compliant to this standard.

2. References

This standard shall be used in conjunction with the following publication. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1364™-2001, IEEE Standard Verilog Language Reference Manual.[1, 2]

[1]IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (http://standards.ieee.org/).
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