

INTERNATIONAL STANDARD

IEC 62050

First edition
2005-07

IEEE 1076.5™

VHDL Register Transfer Level (RTL) synthesis

© IEEE 2005 — Copyright - all rights reserved

IEEE is a registered trademark in the U.S. Patent & Trademark Office, owned by the Institute of Electrical and Electronics Engineers, Inc.

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland
Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch

The Institute of Electrical and Electronics Engineers, Inc, 3 Park Avenue, New York, NY 10016-5997, USA
Telephone: +1 732 562 3800 Telefax: +1 732 562 1571 E-mail: stds-info@ieee.org Web: www.standards.ieee.org



Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия



CONTENTS

FOREWORD	3
IEEE Introduction	6
1. Overview.....	9
1.1 Scope.....	9
1.2 Compliance to this standard.....	9
1.3 Terminology.....	10
1.4 Conventions	10
2. References.....	11
3. Definitions and acronyms	11
3.1 Definitions	11
3.2 Acronyms	12
4. Predefined types.....	13
5. Verification methodology	13
5.1 Combinational verification	14
5.2 Sequential verification	14
6. Modeling hardware elements.....	15
6.1 Edge-sensitive sequential logic.....	15
6.2 Level-sensitive sequential logic.....	27
6.3 Three-state logic and busses	31
6.4 Combinational logic.....	31
6.5 ROM and RAM memories.....	32
7. Pragmas.....	37
7.1 Attributes	37
7.2 Metacomments.....	54
8. Syntax	55
8.1 Design entities and configurations.....	55
8.2 Subprograms and packages.....	60
8.3 Types.....	64
8.4 Declarations	69
8.5 Specification	75
8.6 Names	77
8.7 Expressions	79
8.8 Sequential statements.....	83
8.9 Concurrent statements.....	89
8.10 Scope and visibility.....	94
8.11 Design units and their analysis	95
8.12 Elaboration.....	96
8.13 Lexical elements	96
8.14 Predefined language environment	96
Annex A (informative) Syntax summary.....	99
Annex B (normative) Synthesis package RTL_ATTRIBUTES.....	118
Annex C (informative) List of Participants.....	119
Index	120

INTERNATIONAL ELECTROTECHNICAL COMMISSION

VHDL REGISTER TRANSFERT LEVEL (RTL) SYNTHESIS

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
- 6) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC/IEEE 62050 has been processed through IEC technical committee 93: Design automation.

The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076.6-2004	93/212/FDIS	93/217/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives.

The committee has decided that the contents of this publication will remain unchanged until 2019.

Attention!

It should be noted that this International Standard IEC 62050 is totally unrelated to IEC/PAS 62050 despite the identical numbering."

IEC/IEEE Dual Logo International Standards

This Dual Logo International Standard is the result of an agreement between the IEC and the Institute of Electrical and Electronics Engineers, Inc. (IEEE). The original IEEE Standard was submitted to the IEC for consideration under the agreement, and the resulting IEC/IEEE Dual Logo International Standard has been published in accordance with the ISO/IEC Directives.

IEEE Standards documents are developed within the IEEE Societies and the Standards Coordinating Committees of the IEEE Standards Association (IEEE-SA) Standards Board. The IEEE develops its standards through a consensus development process, approved by the American National Standards Institute, which brings together volunteers representing varied viewpoints and interests to achieve the final product. Volunteers are not necessarily members of the Institute and serve without compensation. While the IEEE administers the process and establishes rules to promote fairness in the consensus development process, the IEEE does not independently evaluate, test, or verify the accuracy of any of the information contained in its standards.

Use of an IEC/IEEE Dual Logo International Standard is wholly voluntary. The IEC and IEEE disclaim liability for any personal injury, property or other damage, of any nature whatsoever, whether special, indirect, consequential, or compensatory, directly or indirectly resulting from the publication, use of, or reliance upon this, or any other IEC or IEEE Standard document.

The IEC and IEEE do not warrant or represent the accuracy or content of the material contained herein, and expressly disclaim any express or implied warranty, including any implied warranty of merchantability or fitness for a specific purpose, or that the use of the material contained herein is free from patent infringement. IEC/IEEE Dual Logo International Standards documents are supplied "AS IS".

The existence of an IEC/IEEE Dual Logo International Standard does not imply that there are no other ways to produce, test, measure, purchase, market, or provide other goods and services related to the scope of the IEC/IEEE Dual Logo International Standard. Furthermore, the viewpoint expressed at the time a standard is approved and issued is subject to change brought about through developments in the state of the art and comments received from users of the standard.

Every IEEE Standard is subjected to review at least every five years for revision or reaffirmation. When a document is more than five years old and has not been reaffirmed, it is reasonable to conclude that its contents, although still of some value, do not wholly reflect the present state of the art. Users are cautioned to check to determine that they have the latest edition of any IEEE Standard.

In publishing and making this document available, the IEC and IEEE are not suggesting or rendering professional or other services for, or on behalf of, any person or entity. Neither the IEC nor IEEE is undertaking to perform any duty owed by any other person or entity to another. Any person utilizing this, and any other IEC/IEEE Dual Logo International Standards or IEEE Standards document, should rely upon the advice of a competent professional in determining the exercise of reasonable care in any given circumstances.

Interpretations – Occasionally questions may arise regarding the meaning of portions of standards as they relate to specific applications. When the need for interpretations is brought to the attention of IEEE, the Institute will initiate action to prepare appropriate responses. Since IEEE Standards represent a consensus of concerned interests, it is important to ensure that any interpretation has also received the concurrence of a balance of interests. For this reason, IEEE and the members of its societies and Standards Coordinating Committees are not able to provide an instant response to interpretation requests except in those cases where the matter has previously received formal consideration.

Comments for revision of IEC/IEEE Dual Logo International Standards are welcome from any interested party, regardless of membership affiliation with the IEC or IEEE. Suggestions for changes in documents should be in the form of a proposed change of text, together with appropriate supporting comments. Comments on standards and requests for interpretations should be addressed to:

Secretary, IEEE-SA Standards Board, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA and/or General Secretary, IEC, 3, rue de Varembe, PO Box 131, 1211 Geneva 20, Switzerland.

Authorization to photocopy portions of any individual standard for internal or personal use is granted by the Institute of Electrical and Electronics Engineers, Inc., provided that the appropriate fee is paid to Copyright Clearance Center. To arrange for payment of licensing fee, please contact Copyright Clearance Center, Customer Service, 222 Rosewood Drive, Danvers, MA 01923 USA; +1 978 750 8400. Permission to photocopy portions of any individual standard for educational classroom use can also be obtained through the Copyright Clearance Center.

NOTE – Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying patents for which a license may be required by an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

IEEE Standard for VHDL Register Transfer Level (RTL) Synthesis

Sponsor

**Design Automation Standards Committee
of the
IEEE Computer Society**

Approved 25 August 2004

American National Standard Institute

Approved 12 May 2004

IEEE-SA Standards Board

Abstract: This document specifies a standard for use of very high-speed integrated circuit hardware description language (VHDL) to model synthesizable register-transfer level digital logic. A standard syntax and semantics for VHDL register-transfer level synthesis is defined. The subset of the VHDL language, which is synthesizable, is described, and nonsynthesizable VHDL constructs are identified that should be ignored or flagged as errors.

Keywords: hardware description language, logic synthesis, register transfer level (RTL), very high-speed integrated circuit hardware description language (VHDL)

IEEE Introduction

This standard describes a standard syntax and semantics for VHDL RTL synthesis. It defines the subset of IEC/IEEE 61691-1-1:2004 (VHDL) that is suitable for RTL synthesis and defines the semantics of that subset for the synthesis domain. This standard is based on IEC/IEEE 61691-1-1:2004, IEEE Std 1164TM-1993, and IEEE Std 1076.3TM-1997.

The purpose of this standard is to define a syntax and semantics that can be used in common by all compliant RTL synthesis tools to achieve uniformity of results in a similar manner to which simulation tools use IEC/IEEE 61691-1-1:2004. This will allow users of synthesis tools to produce well-defined designs whose functional characteristics are independent of a particular synthesis implementation by making their designs compliant with this standard.

The standard is intended for use by logic designers and electronic engineers.

This document specifies IEEE Std 1076.6-2004, which is a revision of IEEE Std 1076.6-1999. The VHDL Synthesis Interoperability Working Group (SIWG) of the IEEE Computer Society started the development of IEEE Std 1076.6-2004 in January 1998. The work initially started as a Level 2 effort (Level 1 being IEEE Std 1076.6-1999). In fact the work on Level 2 continued right after Level 1 was completed by the working group. The working group realized that a Level 2 was required and that it would take some time to develop and continued working on it at regular face-to-face meetings and teleconferences. As the Level 2 draft continued to mature, the working group decided that rather than having two different levels of synthesis subsets, it was better to just have one standard, with IEEE Std 1076.6-2004 becoming Level 2.

The intent of this version was to include a maximum subset of VHDL that could be used to describe synthesizable RTL logic. This included considering new features introduced by IEC/IEEE 61691-1-1:2004, new semantics based on algorithmic styles rather than template-driven, and a set of synthesis attributes that could be used to annotate an RTL description. The following team leaders drove this effort:

Syntax: Lance Thompson

Semantics: Vinaya Singh

Attributes: Sanjiv Narayan

In addition, the following provided much-needed additional support:

Web and reflector admin: David Bishop

Documentation: John Michael Williams

A majority of the work conducted by the working group was done via teleconferencing, which was held regularly and open to all. Also, the working group used an e-mail reflector and its web page effectively to distribute and share information.

The following volunteers contributed to the development of this standard:

J. Bhasker, *Chair*

Jim Lewis, *Vice-Chair*

Rob Anderson	Rich Hatcher	Jonas Nilsson
Bill Anker	Mohammad Kakoe	Alain Raynaud
Victor Berman	Masamichi Kawarabayashi	Mehrdad Reshadi
David Bishop	Apurva Kalia	Fredj Rouatbi
Dominique Borrione	Satish Kumar	Steve Schultz
Dennis Brophy	Evan Lavelle	Manish Shrivastava
Andrew Brown	Vijay Madiseti	Vinaya Singh
Patrick Bryant	Erich Marschner	Douglas Smith
Ben Cohen	Paul Menchini	Lance Thompson
Tim Davis	Amitabh Menon	Alessandro Uber
Colin Dente	Egbert Molenkamp	Jim Vellenga
Wolfgang Ecker	Bob Myers	Eugenio Villar
Bob Flatt	Sanjana Nair	John Michael Williams
Christopher Grimm	Sanjiv Narayan	Francisco De Ycaza
Steve Grout	Zain Navabi	Alex Zamfirescu

Development of IEEE Std 1076.6-1999

Initial work on this standard started as a synthesis interoperability working group under VHDL International. The working group was also chartered by the EDA Industry Council Project Technical Advisory Board (PTAB) to develop a draft based on the donated subsets by the following companies/groups:

- Cadence
- European Synthesis Working Group
- IBM
- Mentor Graphics
- Synopsys

After the PTAB approved of the draft 1.5 with an overwhelming affirmative response, an IEEE PAR was obtained to clear its way for IEEE standardization. Most of the members of the original group continued to be part of the Pilot Group under P1076.6 to lead the technical work.

At the time the 1999 standard was completed, the P1076.6 Pilot Team had the following membership:

Rob Anderson	Wolfgang Ecker	Doug Perry
Victor Berman	Bob Flatt	Steve Schultz
J. Bhasker	Christopher Grimm	Doug Smith
David Bishop	Rich Hatcher	Lance Thompson
Dominique Borrione	Apurva Kalia	Fur-Shing Tsai
Dennis Brophy	Masamichi Kawarabayashi	Jim Vellenga
Ben Cohen	Jim Lewis	Eugenio Villar
Colin Dente	Sanjiv Narayan	Nels Vander Zanden

Many individuals from different organizations contributed to the development of this standard. In particular, in addition to the Pilot Team, the following individuals contributed to the development of the standard by being part of the working group:

Bill Anker	Robert Blackburn	John Hillawi
LaNae Avra		Pradip Jha

In addition, 95 individuals on the working group e-mail reflector also contributed to this development.

Notice to users

Errata

Errata, if any, for this and all other standards can be accessed at the following URL: <http://standards.ieee.org/reading/ieee/updates/errata/index.html>. Users are encouraged to check this URL for errata periodically.

Interpretations

Current interpretations can be accessed at the following URL: <http://standards.ieee.org/reading/ieee/interp/index.html>.

Patents

Attention is called to the possibility that implementation of this standard may require use of subject matter covered by patent rights. By publication of this standard, no position is taken with respect to the existence or validity of any patent rights in connection therewith. The IEEE shall not be responsible for identifying patents or patent applications for which a license may be required to implement an IEEE standard or for conducting inquiries into the legal validity or scope of those patents that are brought to its attention.

VHDL REGISTER TRANSFER LEVEL (RTL) SYNTHESIS

1. Overview

1.1 Scope

This standard defines a subset of very high-speed integrated circuit hardware description language (VHDL) that ensures portability of VHDL descriptions between register transfer level synthesis tools. Synthesis tools may be compliant and yet have features beyond those required by this standard. This standard defines how the semantics of VHDL shall be used, for example, to model level-sensitive and edge-sensitive logic. It also describes the syntax of the language with reference to what shall be supported and what shall not be supported for interoperability.

Use of this standard should minimize the potential for functional simulation mismatches between models before they are synthesized and after they are synthesized.

1.2 Compliance to this standard

1.2.1 Model compliance

A VHDL model shall be defined as being compliant to this standard if the model

- a) Uses only constructs described as supported or ignored in this standard
- b) Adheres to the semantics defined in this standard

1.2.2 Tool compliance

A synthesis tool shall be defined as being compliant to this standard if it

- a) Accepts all models that adhere to the model compliance definition defined in 1.2.1
- b) Supports language related pragmas defined by this standard
- c) Produces a circuit model that has the same functionality as the input model based on the verification process as outlined in Clause 5.

1.3 Terminology

The word *shall* indicates mandatory requirements strictly to be followed in order to conform to the standard and from which no deviation is permitted (*shall* equals *is required to*). The word *should* is used to indicate that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*). The word *may* indicates a course of action permissible within the limits of the standard (*may* equals *is permitted*).

A synthesis tool is said to *accept* a VHDL construct if it allows that construct to be legal input; it is said to *interpret* the construct (or to provide an *interpretation* of the construct) by producing something that represents the construct. A synthesis tool is not required to provide an interpretation for every construct that it accepts, but only for those for which an interpretation is specified by this standard.

The constructs in the standard shall be categorized as follows:

Supported: RTL synthesis shall interpret a construct, that is, map the construct to an equivalent hardware representation.

Ignored: RTL synthesis shall ignore the construct and produce a warning. Encountering the construct shall not cause synthesis to fail, but synthesis results may not match simulation results. The mechanism, if any, by which RTL synthesis notifies (warns) the user of such constructs is not defined by this standard. Ignored constructs may include unsupported constructs.

Not Supported: RTL synthesis does not support the construct. RTL synthesis does not expect to encounter the construct, and the failure mode shall be undefined. RTL synthesis may fail upon encountering such a construct. Failure is not mandatory; more specifically, RTL synthesis is allowed to treat such a construct as ignored.

NOTE—A synthesis tool may interpret constructs that are identified as not supported in this standard. However a model that contains such unsupported constructs is not compliant with this standard.¹

1.4 Conventions

This standard uses the following conventions:

- a) The body of the text of this standard uses **boldface** to denote VHDL reserved words (such as **downto**).
- b) The text of the VHDL examples and code fragments is represented in a fixed-width font.
- c) Syntax text that is struck-through (e.g., ~~text~~) refers to syntax that shall not be supported.
- d) Syntax text that is underscored (e.g., text) refers to syntax that shall be ignored.
- e) < and > pairs are used to represent text in one of several different, but specific forms. For example, one of the forms of <clock_edge> could be “CLOCK'EVENT and CLOCK = '1”.
- f) Any paragraph starting with “NOTE—” is informative and not part of the standard.
- g) The examples that appear in this document under “*Example:*” are for the sole purpose of demonstrating the syntax and semantics of VHDL for synthesis. It is not the intent of this standard to demonstrate, recommend, or emphasize coding styles that are more (or less) efficient in generating an equivalent hardware representation. In addition, it is not the intent of this standard to present examples that represent a compliance test suite, or a performance benchmark, even though these examples are compliant to this standard (except as noted otherwise).

¹Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

2. References

This standard shall be used in conjunction with the following publications. When the following standards are superseded by an approved revision, the revision shall apply.

IEEE Std 1076.3TM-1997, IEEE Standard Synthesis Packages (NUMERIC_BIT and NUMERIC_STD).^{2, 3}

IEEE Std 1164TM-1993, IEEE Standard Multivalued Logic System for VHDL Model Interoperability (STD_LOGIC_1164).

IEC/IEEE 61691-1-1:2004, Behavioural languages - Part 1-1: VHDL language reference manual⁴

²The IEEE standards or products referred to in this clause are trademarks of the Institute of Electrical and Electronics Engineers, Inc.

³IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (<http://standards.ieee.org/>).

⁴IEC/IEEE publications are also available from the Institute of Electrical and Electronics Engineers.