INTERNATIONAL STANDARD

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Behavioural languages –

Part 2: VHDL multilogic system for model interoperability

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

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International Standard IEC 61691-2 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std 1164-1993: *Multivalue logic system for VHDL model interoperability*

The text of this standard is based on the following documents:

FDIS	Report on voting
93/130/FDIS	93/140/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.

IEC 61691 consists of the following parts, under the general title: *Behavioural languages:*

IEC 61691-1:1997, VHDL language reference manual [1)]

IEC 61691-2:2001, Part 2: VHDL multilogic system for model interoperability

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1) The edition 2 with the title: VHSIC hardware description languageVHDL (076a) (under consideration) will replace it.

IEC 61691-3-1, Part 3-1: Analog description in VHDL (under consideration)

IEC 61691-3-2:2001, Part 3-2: Mathematical operation in VHDL

IEC 61691-3-3:2001, Part 3-3: Synthesis in VHDL

IEC 61691-3-4, Part 3-4: Timing expressions in VHDL (under consideration)

IEC 61691-3-5, Part 3-5: Library utilities in VHDL (under consideration)

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

BEHAVIOURAL LANGUAGES - Part 2: VHDL multilogic system for model interoperatibility

1. Overview

1.1 Scope

This standard is embodied in the Std_logic_1164 package package body along with this clause 1 documentation. The information annex AA is a guide to users and is not part of this standard, but suggests ways in which one might use