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Behavioural languages –

Part 1-1:
VHDL language reference manual

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CONTENTS

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BEHAVIOURAL LANGUAGES –

Part 1-1: VHDL language reference manual

FOREWORD

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The text of this standard is based on the following documents:

IEEE Std	FDIS	Report on voting
1076 (2002)	93/193/FDIS	93/198/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives.

The committee has decided that the contents of this publication will remain unchanged until 2007.

IEC 61691 consists of the following parts, under the general title *Behavioural languages:*

IEC/IEEE 61691-1-1, Part 1-1: *VHDL language reference manual*

IEC 61691-2, Part 2: *VHDL multilogic system for model interoperability*

IEC 61691-3-1, Part 3-1: *Analog description in VHDL* (under consideration)

IEC 61691-3-2, Part 3-2: *Mathematical operation in VHDL*

IEC 61691-3-3, Part 3-3: *Synthesis in VHDL*

IEC 61691-3-4, Part 3-4: *Timing expressions in VHDL* (under consideration)

IEC 61691-3-5, Part 3-5: *Library utilities in VHDL* (under consideration)

IEC/IEEE 61691-4, Part 4: *Verilog® hardware description language*

IEC/IEEE 61691-5, Part 5: *VITAL ASIC (application specific integrated circuit) modeling specification*

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IEEE Standard VHDL

Language Reference Manual

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 26 July 2002
American National Standards Institute

Approved 21 March 2002
IEEE-SA Standards Board

Abstract: VHSIC Hardware Description Language (VHDL) is defined. VHDL is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware. Its primary audiences are the implementors of tools supporting the language and the advanced users of the language.
Keywords: computer languages, electronic systems, hardware, hardware design, VHDL

IEEE Introduction

The VHSIC Hardware Description Language (VHDL) is a formal notation intended for use in all phases of the creation of electronic systems. Because it is both machine readable and human readable, it supports the development, verification, synthesis, and testing of hardware designs; the communication of hardware design data; and the maintenance, modification, and procurement of hardware.

This document specifies IEEE Std 1076-2002™, which is a revision of IEEE Std 1076, 2000 Edition™. This revision incorporates the addition of protected types and enhancements to the specification of shared variables which were completed in IEEE Std 1076, 2000 Edition™. As VHDL is now in wide use throughout the world, the 1076 Working Group endeavored to maintain a high level of stability with this revision. Although this revision does not provide significant changes to VHDL, it does enhance and clarify the language specification in several areas. Most notable is the improvement in the specification of default binding rules, buffer ports, scope and visibility, allowance of multi-byte characters in comments and other areas which will increase the portability of descriptions.

The maintenance of the VHDL language standard is an ongoing process. The chair of the VHDL Analysis and Standardization Group (VASG), otherwise known as the 1076 Working Group, extends his gratitude to all who have participated in this revision and encourages the participation of all interested parties in future language revisions. If interested in participating, please contact the VASG at stds-vasg@ieee.org or visit the following website: http://www.eda.org/pub/vasg.

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BEHAVIOURAL LANGUAGES –

Part 1-1: VHDL language reference manual

0. Overview of this standard

This clause describes the purpose and organization of this standard, the IEEE Standard VHDL Language Reference Manual.

0.1 Intent and scope of this standard

The intent of this standard is to define VHSIC Hardware Description Language (VHDL) accurately. Its primary audiences are the implementor of tools supporting the language and the advanced user of the language. Other users are encouraged to use commercially available books, tutorials, and classes to learn the language in some detail prior to reading this standard. These resources generally focus on how to use the language, rather than how a VHDL-compliant tool is required to behave.

At the time of its publication, this document was the authoritative definition of VHDL. From time to time, it may become necessary to correct and/or clarify portions of this standard. Such corrections and clarifications may be published in separate documents. Such documents modify this standard at the time of their publication and remain in effect until superseded by subsequent documents or until the standard is officially revised.

0.2 Structure and terminology of this standard

This standard is organized into clauses, each of which focuses on some particular area of the language. Within each clause, individual constructs or concepts are discussed in each subclause.

Each subclause describing a specific construct begins with an introductory paragraph. Next, the syntax of the construct is described using one or more grammatical *productions*.

A set of paragraphs describing the meaning and restrictions of the construct in narrative form then follow. Unlike many other IEEE standards, which use the verb *shall* to indicate mandatory requirements of the standard and *may* to indicate optional features, the verb *is* is used uniformly throughout this document. In all cases, *is* is to be interpreted as having mandatory weight.

Additionally, the word *must* is used to indicate mandatory weight. This word is preferred over the more common *shall*, as *must* denotes a different meaning to different readers of this standard.

a) To the developer of tools that process VHDL, *must* denotes a requirement that the standard imposes. The resulting implementation is required to enforce the requirement and to issue an error if the requirement is not met by some VHDL source text.

b) To the VHDL model developer, *must* denotes that the characteristics of VHDL are natural consequences of the language definition. The model developer is required to adhere to the constraint implied by the characteristic.

c) To the VHDL model user, *must* denotes that the characteristics of the models are natural consequences of the language definition. The model user can depend on the characteristics of the model implied by its VHDL source text.

Finally, each clause may end with examples, notes, and references to other pertinent clauses.

0.2.1 Syntactic description

The form of a VHDL description is described by means of context-free syntax using a simple variant of the backus naur form; in particular:

a) Lowercase words in roman font, some containing embedded underlines, are used to denote syntactic categories, for example:

formal_port_list

Whenever the name of a syntactic category is used, apart from the syntax rules themselves, spaces take the place of underlines (thus, “formal port list” would appear in the narrative description when referring to the above syntactic category).

b) Boldface words are used to denote reserved words, for example:

array

Reserved words must be used only in those places indicated by the syntax.

c) A *production* consists of a *left-hand side*, the symbol “::=” (which is read as “can be replaced by”), and a *right-hand side*. The left-hand side of a production is always a syntactic category; the right-hand side is a replacement rule. The meaning of a production is a textual-replacement rule: any occurrence of the left-hand side may be replaced by an instance of the right-hand side.

d) A vertical bar (|) separates alternative items on the right-hand side of a production unless it occurs immediately after an opening brace, in which case it stands for itself, as follows:

letter_or_digit ::= letter | digit
choices ::= choice { | choice }

In the first instance, an occurrence of “letter_or_digit” can be replaced by either “letter” or “digit.” In the second case, “choices” can be replaced by a list of “choice,” separated by vertical bars [see item f) for the meaning of braces].

e) Square brackets [ ] enclose optional items on the right-hand side of a production; thus, the following two productions are equivalent:

return_statement ::= **return** [expression] ;
return_statement ::= **return** ; | **return** expression ;

Note, however, that the initial and terminal square brackets in the right-hand side of the production for signatures (see 2.3.2) are part of the syntax of signatures and do not indicate that the entire right-hand side is optional.

f) Braces { } enclose a repeated item or items on the right-hand side of a production. The items may appear zero or more times; the repetitions occur from left to right as with an equivalent left-recursive rule. Thus, the following two productions are equivalent:

term ::= factor { multiplying_operator factor }
term ::= factor | term multiplying_operator factor

g) If the name of any syntactic category starts with an italicized part, it is equivalent to the category name without the italicized part. The italicized part is intended to convey some semantic information. For example, *type*_name and *subtype*_name are both syntactically equivalent to name alone.

h) The term simple_name is used for any occurrence of an identifier that already denotes some declared entity.

0.2.2 Semantic description

The meaning and restrictions of a particular construct are described with a set of narrative rules immediately following the syntactic productions. In these rules, an italicized term indicates the definition of that term and identifiers appearing entirely in uppercase letters refer to definitions in package STANDARD (see 14.2).

The following terms are used in these semantic descriptions with the following meanings:

erroneous: The condition described represents an ill-formed description; however, implementations are not required to detect and report this condition. Conditions are deemed erroneous only when it is impossible in general to detect the condition during the processing of the language.

error: The condition described represents an ill-formed description; implementations are required to detect the condition and report an error to the user of the tool.

illegal: A synonym for “error.”

legal: The condition described represents a well-formed description.

0.2.3 Front matter, examples, notes, references, and annexes

Prior to this subclause are several pieces of introductory material; following Clause 14 are some annexes and an index. The front matter, annexes, and index serve to orient and otherwise aid the user of this standard, but are not part of the definition of VHDL.

Some clauses of this standard contain examples, notes, and cross-references to other clauses of the standard; these parts always appear at the end of a clause. Examples are meant to illustrate the possible forms of the construct described. Illegal examples are italicized. Notes are meant to emphasize consequences of the rules described in the clause or elsewhere. In order to distinguish notes from the other narrative portions of this standard, notes are set as enumerated paragraphs in a font smaller than the rest of the text. Cross-references are meant to guide the user to other relevant clauses of the standard. Examples, notes, and cross-references are not part of the definition of the language.