INTERNATIONAL STANDARD

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Delay and power calculation standards –

Part 2:
pre-layout delay calculation specification for CMOS ASIC libraries

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61523-2 has been prepared by IEC technical committee 93: Design automation.

The ASIC Library Representation Working Group of EIAL EDA Technical Committee also participated in the preparation of this standard.

This standard is a revision of the EIAJ[1] document: *ASIC Library Representation (ALR):1994.*

The text of this standard is based on the following documents:

FDIS	Report on voting
93/151/FDIS	93/153/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 2 of the ISO/IEC Directives.

NOTE This standard has been reproduced without significant modification of its original content or drafting.

[1] Electronic Industries Association of Japan.

IEC 61523 consists of the following parts, under the general title: *Delay and calculation standards:*

IEC 61523-1:2001, Part 1: *Integrated circuit delay and power calculation systems*

IEC 61523-2, Part 2: *Pre-layout delay calculation specification for CMOS ASIC libraries*

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

DELAY AND CALCULATION STANDARDS –

Part 2: Pre-layout delay calculation specification for CMOS ASIC libraries

1. Scope and object

This standard specifies the pre-layout delay calculation method for CMOS1[1)]ASIC[2)] Libraries which contains cell based primitives and memories to be used during the pre-layout design phase of Logic simulation, Timing verification, and Logic synthesis.
The delay calculation method addressed in this standard consists of
1) Estimation of wire capacitance and
2) Delay calculation method based on tablelook-up.
With use of DCL and SDF, this delay calculation method helps the user have a unified timing model for various EDA tools in the pre-layout design phase.

This standard is consistent with existing standards and accepts existing standard formats, like SPEF, DCL, and SDF.
Scope of this standard covers the CMOS ASIC front end timing design for using logic synthesizer, simulators, timing verifiers.
The delay calculation method specified is based on the input slew rate calculation step and the port to port calculation step.
During these calculation steps, the table lookup method is used.
The table method of this standard specifies two interpolation methods for delay calculation. One is bi-linear interpolation which is widely used through the industry. Another is a linear interpolation using neighboring 3 points.
The nature of the delay value has monotonously increasing function of convex surface. This linear interpolation has a few percent of differences between linear interpolation and SPICE result.

2. Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies

IEEE Standard 1481:1999, *Integrated Circuit (IC) Delay and Power Calculation System.*

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1) Complementary metal oxide semiconductor (CMOS).
2) Application – Specific Integrated Circuits (ASIC).