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Delay and power calculation standards –

Part 1:
Integrated circuit delay and power calculation systems

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FOREWORD

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International Standard IEC 61523-1 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std P1481 (1999): *IEEE Standard for delay and power calculation systems.*

The text of this standard is based on the following documents:

FDIS	Report on voting
93/143/FDIS	93/144/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.

IEC 61523 consists of the following parts, under the general title: *Delay and calculation standards:*

IEC 61523-1, Part 1: *Integrated circuit delay and power calculation systems*

IEC 61523-2, Part 2: *Prelayout delay calculation model specification of CMOS ASIC libraries* (to be published)

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

Introduction

The objective of the Delay and Power Calculation System (DPCS) is to make it possible for integrated circuit designers to *consistently* calculate chip delay and power across Electronic Design Automation (EDA) applications and for integrated circuit vendors to express delay and power information only *once* per technology while enabling sufficient EDA application accuracy.

This is accomplished by a coordinated set of standards which support a standard method to describe timing and power characteristics of integrated circuit design units (cells and higher level design elements); a standard method for EDA applications to calculate chip design instance specific delay, slew, and power for logic and interconnects; and standard file formats to exchange chip parasitic and cluster information.

A major integrated circuit design problem is to ensure the chip meets the designer's timing and power requirements. At this time in the EDA industry, there are numerous methodologies — many incompatible or inconsistent with each other — for representing timing and power information. The DPCS responds to the urgency to improve chip design methods.

The DPCS includes all aspects and uses of delay and power calculation (including synthesis, floorplanning, and simulation) during both pre-layout and post-layout phases of chip design. A fundamental requirement placed on the DPCS is that it work equally well with Verilog HDL and VHDL. In this draft of the standard, the scope of the DPCS is limited to integrated circuit designs.

The DPCS gains its leverage out of an effort by Silicon Integration Initiative (Si2) to standardize on contributed technology from IBM in the form of a Delay Calculation Language (DCL) and its companion procedural interface (PI), along with an effort by Open Verilog International (OVI) to standardize on file formats to exchange chip parasitic and cluster information in the form of a Physical Design Exchange Format (PDEF) and a Standard Parasitic Exchange Format (SPEF). SPEF is based on the Standard Parasitic Format (SPF) technology supplied by Cadence Design Systems. PDEF is based on technology provided by Synopsys.

Since each of these specifications is based on existing technology which has proven itself in industry, the time to introduce this standard into industry is greatly reduced over what would have been required for a newly created standard. The industry owes a great deal of gratitude to these companies for contributing these technologies.

The P1481 Working Group is composed of four subgroups: Architecture, Language, Parasitics and Clustering, and Power. The members of each of these groups are members of the P1481 Working Group. The P1481 Working Group has a vice-chair liaison with Japan to coordinate development and review of the specification there. The IEC TC93 WG 2 also participates in the review and development of this specification.

In addition to numerous individual contributors, both OVI, VHDL International (VI), and Si2 have played significant roles in the development of this standard and funding of the technical documentation.

DELAY AND POWER CALCULATION STANDARDS –

Part 1: Integrated circuit delay and power calculation systems

1. Overview

The Delay and Power Calculation System (DPCS) standard is a coordinated set of standards which support a standard method to describe timing and power characteristics of integrated circuit design units (cells and higher level design elements); a standard method for EDA applications to calculate chip design instance specific delay, slew, and power for logic and interconnects; and standard file formats to exchange chip parasitic and cluster information. The four distinct standard specifications covered in this document include:

- A description language for timing and power modeling (DCL).
- A software procedural interface (PI) for communications between EDA applications and compiled libraries of DCL descriptions.
- A standard file exchange format for parasitic information about the chip design (SPEF).
- A standard file exchange format for floorplan cluster information relative to the chip design (PDEF).

1.1 Scope

As stated in the introduction, the scope of the DPCS standard is to make it possible for integrated circuit designers to analyze chip timing and power consistently across a broad set of EDA applications, for integrated circuit vendors to express timing and power information once (for a given technology), and for EDA vendors to meet their application performance and capacity needs. The intended use for these standards is integrated circuit timing and power. The standard may be applied to both unit logic cells supplied by the integrated circuit vendor and logical macros defined by the integrated circuit designer. Although this specification is written towards the integrated circuit supplier and EDA developer, its application applies equally well to representation of timing and power for designer defined macros (or hierarchical design elements).

These specifications make it *possible* to achieve consistent timing and power results, but do not *guarantee* it. They provide for a single executable software program which computes delay and power based on integrated circuit vendor-supplied algorithms (or designer-supplied algorithms for macros), but does not guarantee EDA applications correctly communicate the design-specific information required for these algorithms. By specifying standard exchange formats for parasitic data and floorplanning information, the standard provides a marked improvement over design environments with no such standards. However, it is the responsibility of the EDA application to correctly correlate the information between these standard exchange files and the actual design. These specifications also do not detail how the information contained within the standard exchange files shall be obtained.