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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Test methods for electrical materials, printed boards and other interconnection structures and assemblies – Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling

Méthodes d'essai pour les matériaux électriques, les cartes imprimées et autres structures d'interconnexion et ensembles – Partie 3-719: Méthodes d'essai pour les structures d'interconnexion (cartes imprimées) – Contrôles de la variation de résistance des trous métallisés uniques (PTH) au cours des cycles de températures

IEC Central Office
3, rue de Varembé
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
Fax: +41 22 919 03 00
info@iec.ch
www.iec.ch

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling

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International Standard IEC 61189-3-719 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/1303/FDIS	91/1327/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 61189 series, published under the general title *Test methods for electrical materials, printed boards and other interconnection structures and assemblies* can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

TEST METHODS FOR ELECTRICAL MATERIALS, PRINTED BOARDS AND OTHER INTERCONNECTION STRUCTURES AND ASSEMBLIES –

Part 3-719: Test methods for interconnection structures (printed boards) – Monitoring of single plated-through hole (PTH) resistance change during temperature cycling

1 Scope

This part of IEC 61189 specifies a test method to monitor the resistance of single plated-through holes (PTHs) in printed circuit boards (PCBs) to determine the PTH durability under thermo-mechanical stress induced by temperature cycling.

2 Normative references

The following documents, in whole or in part, are normatively referenced in this document and are indispensable for its application. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-14, *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*

IEC 60068-2-58:2015, *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60194, *Printed board design, manufacture and assembly – Terms and definitions*

IPC-2221, *Generic Standard on Printed Board Design*

3 Terms and definitions

For the purposes of this document the terms and definitions given in IEC 60194 apply, unless otherwise specified.

4 Test specimens

The test panels are coupons of N layer PCBs (see Figure 1 for an example of a section of a test coupon for a six-layer PCB).

If not described in the relevant specification, one test coupon shall have:

- four single through-holes connecting from the first (top, outer) to the N^{th} (bottom, outer) layer (via L1 – via LN) with the corresponding labelling;
- four single through-holes connecting from the second to the third layer (via L2 – via L3) or the (N2) to the (N1) layers with the corresponding labelling;
- one reference conductive pattern on an outer layer to compensate for possible temperature fluctuations over different temperature cycles and for resistance changes of the conductors by ageing during the test. The length of the reference structure conductive pattern is not relevant, but it is recommended to use a length similar to the length of the conductive patterns connecting the vias to the connection points (see Figure 1) and to