IEC 61188-5-8

Edition 1.0 2007-10

INTERNATIONAL STANDARD

Printed boards and printed board assemblies – Design and use –
Part 5-8: Attachment (land/joint) considerations – Area array components (BGA, FBGA, CGA, LGA)

INTERNATIONAL
ELECTROTECHNICAL
COMMISSION

PRICE CODE U

ICS 31.180

ISBN 2-8318-9343-7

CONTENTS

INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 5-8: Attachment (land/joint) considerations – Area array components (BGA, FBGA, CGA, LGA)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 61188-5-8 has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this standard is based on the following documents:

FDIS	Report on voting
91/705/FDIS	91/737/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

IEC 61188-5-8 is to be read in conjunction with IEC 61188-5-1.

A list of all parts of the IEC 61188 series, under the general title *Printed boards and printed board assemblies – Design and use*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

This part of IEC 61188 covers land patterns for area array components which include ball grid array (BGA) parts (rigid, flexible or ceramic substrate); fine pitch ball grid array (FBGA) parts (rigid or flexible substrate); column grid array (CGA) parts (ceramic substrates) and land grid array (LGA) parts (ceramic substrates). Each clause contains information in accordance with the area array family of components and their requirements for appropriate land patterns.

The proposed land pattern dimensions in this standard are based upon the fundamental tolerance calculation combined with the given land geometries and courtyard excesses (see IEC 61188-5-1, Generic requirements). The courtyard includes all issues of the normal manufacturing necessities.

The unaltered land pattern dimensions of this part are generally applicable for the solder paste application plus the reflow soldering process.

Although other standards in the IEC 61188-5 series define three levels of land pattern dimensioning, this standard will only define two levels. One level (level 2) is for non collapsing BGA balls; the other level (level 3) is for those BGA components where the ball does collapse around the land. All land descriptions are non-solder mask defined. Each land pattern has been assigned an identification number to indicate the characteristics of the specific robustness of the land patterns. Users also have the opportunity to organize the information so that it is most useful for their particular design.

If a user has good reason to use a concept different from that of IEC 61188-5-1, or if the user prefers unusual land geometries, this standard should be used for checking the resulting ball to land relationship.

It is the responsibility of the user to verify the SMD land patterns used for achieving an undisturbed mounting process including testing and an ensured reliability for the product stress conditions in use. In addition, the size and shape of the proposed land pattern may vary according to the solder resist aperture, the size of the land pattern extension (dog bone), the via within the extension, or if the via is in the land pattern itself.

Dimensions of the components listed in this standard are of those available in the market, and regarded as reference only.

PRINTED BOARDS AND PRINTED BOARD ASSEMBLIES – DESIGN AND USE –

Part 5-8: Attachment (land/joint) considerations – Area array components (BGA, FBGA, CGA, LGA)

1 Scope

This part of IEC 61188 provides information on land pattern geometries used for the surface attachment of electronic components with area array terminations in the form of solder balls, solder columns or protective coated lands. The intent of the information presented herein is to provide the appropriate size, shape and tolerances of surface mount land patterns to ensure sufficient area for the appropriate solder joint, and also allow for inspection, testing and reworking of those solder joints.

Each clause contains a specific set of criteria such that the information presented is consistent, providing information on the component, the component dimensions, the solder joint design and the land pattern dimensions.

The land pattern dimensions are based on a mathematical model that establishes a platform for a solder joint attachment to the printed board. The existing models create a platform that is capable of establishing a reliable solder joint no matter which solder alloy is used to make that joint (lead-free, tin lead, etc.).

Process requirements for solder reflow are different depending on the solder alloy and should be analyzed so that the process is taking place above the liquidus temperature of the alloy, and remains above that temperature a sufficient time to form a reliable metallurgical bond.

Area array land patterns do not use "land protrusion" concepts and attempt to match the characteristics of the physical and dimensional termination properties. There are several configurations available, as shown in Figure 1. However, the tables provided show only the optimum dimension across the outer construction of the land.

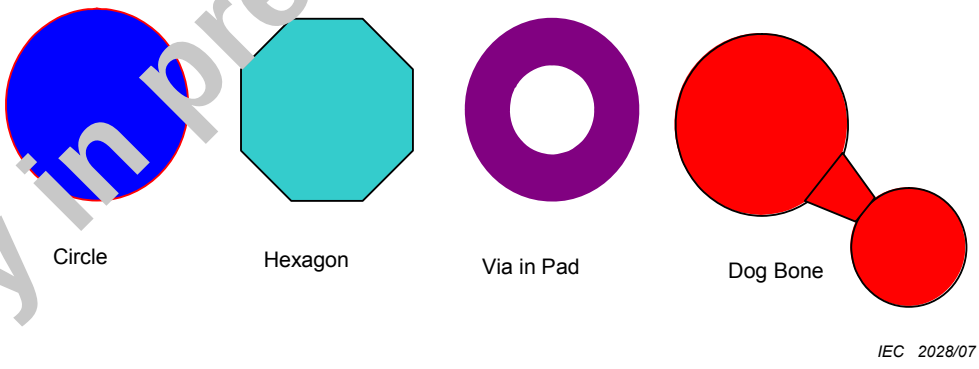

Figure 1 – Area array land pattern configuration

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-58, *Environmental testing – Part 2-58: Tests: Test Td – Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*

IEC 60191-2 (all parts), *Mechanical standardization of semiconductor devices – Part 2: Dimensions*

IEC 61188-5-1, *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*

IEC 62090, *Product package labels for electronic components using bar code and two-dimensional symbologies*