



BSI Standards Publication

Device embedded substrate

Part 2-2: Guidelines — Electrical
testing

National foreword

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TECHNICAL REPORT

RAPPORT TECHNIQUE



**Device embedded substrate –
Part 2-2: Guidelines – Electrical testing**

**Substrat avec appareil(s) intégré(s) –
Partie 2-2: Directives – Essai électrique**

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DEVICE EMBEDDED SUBSTRATE –

Part 2-2: Guidelines – Electrical testing

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IEC TR 62878-2-2, which is a Technical Report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Enquiry draft	Report on voting
91/1220/DTR	91/1245/RVC

Full information on the voting for the approval of this Technical Report can be found in the report on voting indicated in the above table.

The French version of this Technical Report has not been voted upon.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedded substrate*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the stability date indicated on the IEC website under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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INTRODUCTION

Current electrical package designs are becoming more complex, more functionally integrated, more reliable and more miniaturized than ever. Hence, electrical tests should be classified into levels in order to ensure the performance and quality of device embedded substrates since the substrate contains active/passive devices within it. While the interconnection open/short test is enough for general substrates, functional tests should be done when active/passive devices are embedded inside the substrate. However, the main problem is that we need to understand which devices are embedded and how they are connected functionally to each other. This is the main reason that there should be standardized test methods for device embedded substrate. Figure 1 shows the existing substrate test method: the interconnection open/short test.

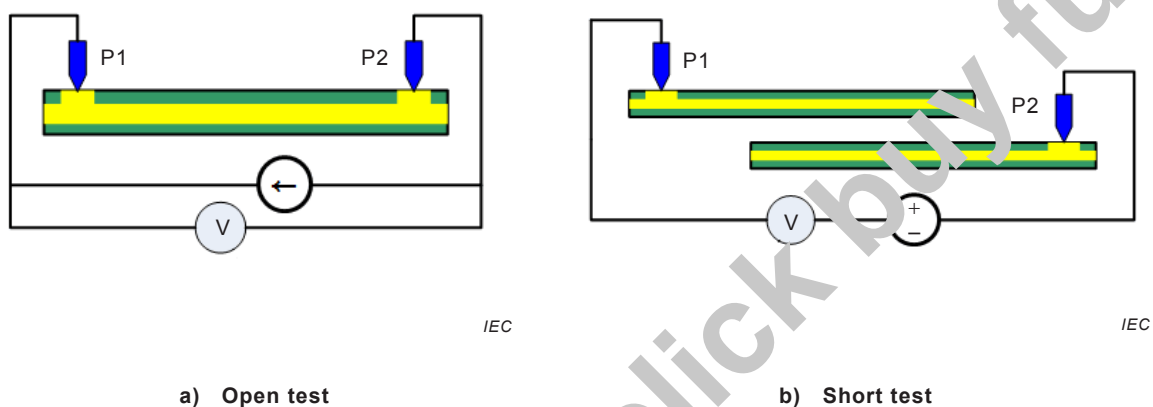


Figure 1 – Interconnection open/short test

DEVICE EMBEDDED SUBSTRATE –

Part 2-2: Guidelines – Electrical testing

1 Scope

This part of IEC 62878, which is a Technical Report, describes the necessary information on electrical testing for device embedded substrate. This includes the interconnection open and short-circuit tests as well as the device functional test. It also provides guidelines by demonstrating the electrical test for device embedded substrate.

This part of IEC 62878 is applicable to device embedded substrates fabricated by use of organic base material, which include for example active or passive devices, discrete components formed in the fabrication process of electronic wiring board, and sheet formed components.

The IEC 62878 series does not apply to the re-distribution layer (RDL) nor to the electronic modules defined as an M-type business model in IEC 62421.

2 Electrical tests

2.1 Test level 1A for device embedded substrate

Test level 1A for device embedded substrate is to check the continuity and isolation of interconnections which are not connected to any embedded components. This is shown in Figure 2. Test point 1 and test point 2 are on different networks. After measuring the resistance between net 1 and net 2, it can be found that net 1 and net 2 are short if the measured resistances are below a certain resistance. Test point 3 and test point 4 are on the same net, which is net 3. They are open if the measured resistance between the two test points is over a certain resistance. It means that they are not electrically connected.

Multi-testers which can measure voltage and current are commercially available. The source meter can measure the resistance directly since it has its own power supply. In terms of reliability, a high-current or high-level voltage test can be done to check the micro-open which causes the latent defects in the printed-circuit board and to check the micro-short which causes noise in the RF system.