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BSI Standards Publication

Device embedding assembly technology

Part 2-8: Guidelines — Warpage control of active device embedded substrate

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National foreword

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The UK participation in its preparation was entrusted to Technical Committee EPL/501, Electronic Assembly Technology.

A list of organizations represented on this committee can be obtained on request to its committee manager.

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Device embedding assembly technology – Part 2-8: Guidelines – Warpage control of active device embedded substrate

INTERNATIONAL ELECTROTECHNICAL COMMISSION

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

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FOREWORD

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IEC TR 62878-2-8, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
91/1649/DTR	91/1721/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/standardsdev/publications.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY –

Part 2-8: Guidelines – Warpage control of active device embedded substrate

1 Scope

This part of IEC 62878 describes a warpage control of active device embedded substrate along with parameters for determining warpage, which are useful during package assembly. Warpage results are explained using warpage driving force, resistance and neutral axis, for typical die embedded substrate, where the discrete active dies are placed in the core of substrate and interconnected to the substrate by direct Cu bonding. The same principles are applicable in other device embedded substrates. Even though the detailed structure of other device embedded substrates might be different, the origin and determination of the parameters of warpage are the same and thus the purpose of this report is to help engineers improve the warpage behaviours of their products by applying this principle.

2 Normative references

IEC 60194 (all parts), *Printed boards design, manufacture and assembly – Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

- IEC Electropedia: available at http://www.electropedia.org/
- ISO Online browsing platform: available at http://www.iso.org/obp

3.1
warpage
deviation from uniform flatness of the substrate for the range of thermal conditions experienced during the package to board assembly

Note 1 to entry: Warpage during board assembly can cause the device terminals to have open or short circuit connections after the reflow soldering operation. Certain package types, such as BGAs (ball grid arrays), have been found to be more susceptible to component warpage [1][1].

Note 2 to entry: Package warpage depends on many factors including CTE mismatch between device constituents, assembly process, package design geometries, top and embedded die, substrate, etc. (x, y, & z). In addition, it can be related with use of IHS (integrated heat spreader), stiffener, or overmold (geometries and material choices include sealant/adhesives used), and other technology aspects of embedded design, embedded and external caps, use of GaA vs. SiO2, etc.

[1] Numbers in square brackets refer to the Bibliography.