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DIAGRAMS, CHARTS AND TABLES FOR ELECTROTECHNOLOGY

Part 8—GUIDING PRINCIPLES FOR THE PREPARATION OF LOGIC DIAGRAMS

STANDARDS ASSOCIATION OF AUSTRALIA
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AUSTRALIAN STANDARD

DIAGRAMS, CHARTS AND TABLES FOR ELECTROTECHNOLOGY

Part 8 GUIDING PRINCIPLES FOR THE PREPARATION OF LOGIC DIAGRAMS

AS 1103.8—1986

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PREFACE

This standard was prepared by the Association's Committee on Symbols, Units and Quantities for Electrotechnology. It is one of the AS 1103 series of standards on diagrams, charts and tables which have been prepared under the authority of both the Telecommunications and Electronics and the Electrical Standards Boards.

The AS 1103 series of standards (of which this standard is Part 8) is complementary with the AS 1100 series (Drawing Practice) and the AS 1102 series (Graphical Symbols for Electrotechnology).

For relevant information on matters specific to drawing practice but which are not covered in the AS 1103 series, reference should be made to the AS 1100 series. In addition, reference may also be required to AS 1046, Letter Symbols for Use in Electrotechnology, Part 1, General, and Part 2, Telecommunications and Electronics.

The standards so far published in the AS 1103 series are listed in the SAA Catalogue of Publications.

The purpose of this standard is to provide recommendations for the preparation of logic diagrams. For this reason, it is recommended that the standard be read in conjunction with AS 1102, Graphical Symbols for Electrotechnology, Part 9—Binary Logic Elements, some aspects of which are included in this standard.

During the preparation of this standard, reference was made to IEC 113-7—1981 Diagrams, Charts and Tables for Electrotechnology, Part 7—Preparation of Logic Diagrams. Although this standard is technically similar to IEC 113-7-1981, it also includes additional examples based on Australian practice. However, the polarity indicator logic convention stated herein is not in common use within Australia.

Attention is also drawn to SAA HB8, Understanding Logic Symbols, a new handbook which explains the development of logic symbols depicted in AS 1102, Part 9.

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Australian Standard
for
DIAGRAMS, CHARTS AND TABLES FOR ELECTROTECHNOLOGY

PART 8—GUIDING PRINCIPLES FOR THE PREPARATION OF LOGIC DIAGRAMS

1 SCOPE. This standard gives recommendations for the preparation of logic diagrams.

NOTE: The AS 1103 series of standards (in particular AS 1103, Part 4), provides additional guidance regarding drawing practice. Graphical symbols for diagrams are given in the AS 1102 series of standards.

2 REFERENCED DOCUMENTS. The following standards are referred to in this standard:

AS 1102 Graphical Symbols for Electrotechnology
Part 9—Binary Logic Elements

AS 1103 Diagrams, Charts and Tables for Electrotechnology
Part 1—Definitions and Classifications
Part 3—Basic Principles for the Presentation of Elements of Electrical Diagrams
Part 4—Guiding Principles for the Preparation of Circuit Diagrams

3 DEFINITIONS. For the purpose of this standard, definitions given in AS 1102, Part 9, AS 1103, Part 1, and the following apply:

3.1 Basic logic diagram—a logic diagram that describes logic functions without reference to physical implementation. It consists primarily of logic symbols and is used to depict all logic relationships as concisely as possible. Non-logic functions are not normally shown.

3.2 Detailed logic diagram—a logic diagram that depicts all logic functions and also shows non-logic functions, connectors, pin numbers, test points, and other elements necessary to describe the physical and electrical aspects of the system.

NOTE: Detailed logic diagrams are used primarily to facilitate the diagnosis and localization of system malfunctions. They are also used to verify the physical consistency of the logic and to prepare instructions. The symbols are generally connected by lines that represent signal paths.

3.3 Table of combinations (truth tables)—a table describing the input/output conditions for a basic logic function.

3.4 Logic convention—a means of defining the logic 1-state and the logic 0-state of a binary digital variable in terms of H (high) and L (low) voltage levels.

NOTE: For detailed information, see Appendix B.

3.5 Positive logic convention—a convention in which the H (high) level of a physical quantity represents the 1-state of a binary digital variable and the L (low) level the 0-state.

3.6 Negative logic convention—a convention in which the H (high) level of a physical quantity represents the 0-state of a binary digital variable and the L (low) level the 1-state.

3.7 Logic polarity indicator—the presence of the logic polarity indicator at a specific input or output signifies that the L-level of the physical quantity corresponds with the logic 1-state. Absence of the indicator at a specific input or output indicates that the H-level corresponds to the 1-state at that point.

4 GRAPHICAL SYMBOLS

4.1 General. Symbols for binary logic elements are given in AS 1102, Part 9.

Symbol size should be governed by the space necessary for internal annotations and the length of the side needed to accommodate input and output lines at an acceptable spacing (see AS 1102, Part 9 and AS 1103, Part 3).

Input and output lines should be placed on two opposite sides of the symbol and shall join the outline of the symbol at right angles. The special rules for complex elements shall be observed (see AS 1102, Part 9).

Most logic diagrams will also require the use of symbols taken from the AS 1102 series of standards.

4.2 Combination of symbols. Rules for combining symbols for basic operations are given in AS 1102, Part 9. Symbols representing hardware elements which are contained in one physical package may also be combined providing the interconnections are not accessible to the user and the rules mentioned above are applied (see AS 1102, Part 9).

4.3 Symbol orientation. The orientation of a symbol does not alter the meaning of that symbol, but the preferred direction of information flow should be from left to right or from top to bottom. Irrespective of symbol orientation, the following rules shall be observed:

(a) In general, connect outputs to the opposite side of the symbols from the inputs.

(b) Obey the rules given in AS 1102, Part 9, for the placement of the qualifying symbol(s) for the device function.

(c) Provide sufficient space to avoid confusion between the qualifying symbol(s) for the function and the input and output labels.

(d) Strings of characters, forming qualifying symbols or labels, should preferably appear in normal reading order. Centre each input (output) label with respect to its input (output) line.

(e) Ensure that the orientation of qualifying symbols for negation, polarity, grouping, dynamic input, non-logic and amplification with respect to the connection lines, is unchanged.

Table 1 gives examples of preferred symbol orientation.